

AP918

Flash Microcontroller with LCD Driver for USB Audio Application

Datasheet

Table of Contents

1. OVERVIEW	1
2. APPLICATIONS	1
2.1. TARGET APPLICATIONS	1
2.2. APPLICATION FEATURES	1
2.2.1 USB AUDIO FEATURE	1
2.2.2 DOCKING CONTROL FEATURES	1
2.2.3 CLOCK AND ALARM FEATURES	1
2.2.4 RADIO FEATURES	1
2.2.5 OTHER SYSTEM FEATURES	1
3. ORDERING INFORMATION	1
4. PIN CONFIGURATION	2
5. BLOCK DIAGRAM	3
6. BUILT-IN PERIPHERALS	4
7. PIN DESCRIPTION	5
8. ELECTRICAL SPECIFICATION	7
8.1. ABSOLUTE MAXIMUM RATING	7
8.2. RECOMMENDED OPERATING CONDITION	7
8.3. LEAKAGE CURRENT AND CAPACITANCE	7
8.4. DC ELECTRICAL CHARACTERISTICS	8
9. PACKAGE INFORMATION	9
10. SOLDERING INDICATION	10
1. REFLOW SOLDERING	10
2. WAVE SOLDERING	10
3. MANUAL SOLDERING	10
4. SUITABILITY OF SURFACE MOUNT IC PACKAGES FOR WAVE AND REFLOW SOLDERING METHODS	11

1. OVERVIEW

The AP918 integrated circuit (IC) is a low-power CMOS 8-bit microcontroller (MCU) for USB audio application with universal serial bus (USB) peripheral interface designed specifically for applications that require isochronous data streaming. Applications include iPod digital docking and PC USB audio.

2. APPLICATIONS

2.1. Target Applications

- Docking system
- Clock radio
- USB audio application
- Bluetooth application

2.2. Application Features

2.2.1 USB Audio Feature

- Playback audio file from iPhone/iPod/iPad through USB interface

2.2.2 Docking Control Features

- Docking control through front panel buttons or remote controller
- Device charging through docking system
- Support Apple Authentication Coprocessor

2.2.3 Clock and Alarm Features

- 12/24 hour clock display mode selectable by user

- Dual alarm clocks
- User selectable alarm mode – wake-to-buzzer, wake-to-radio or wake-to-docked device
- Fixed snooze feature
- Programmable sleep timer

2.2.4 Radio Features

- Auto/Manual radio station scanning
- Programmable radio station memory (independent memory slots for FM and AM)

2.2.5 Other System Features

- Support 40 segment x 2 - 6 common, 1/3 bias LCD display
- Automatic detection of AC power
- Low standby current
- Firmware upgrade

3. ORDERING INFORMATION

ORDERING NUMBER	PINS	PACKAGE
AP918-LQ-L	100	LQFP

4. PIN CONFIGURATION

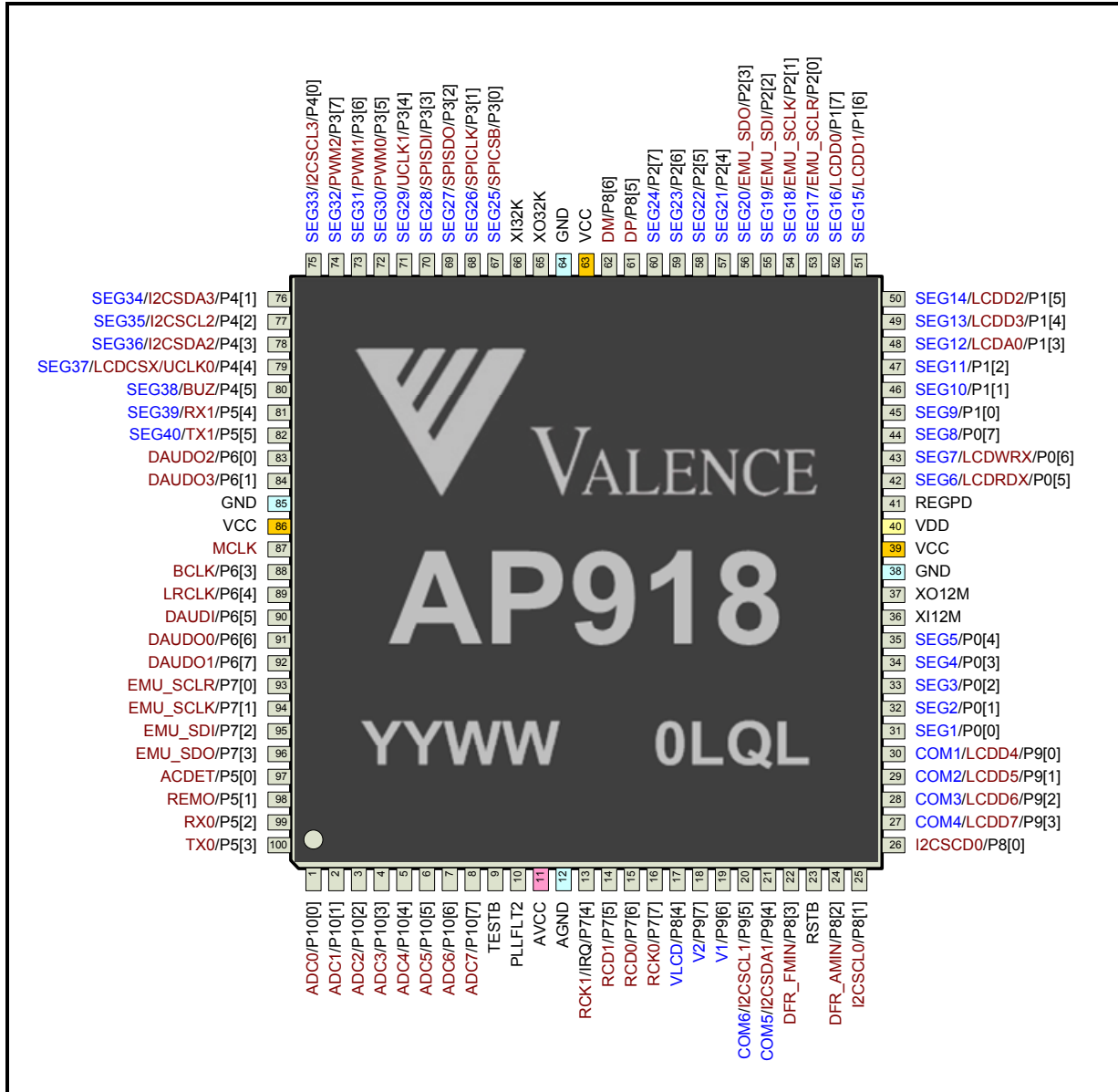


Figure 1 100-Pin LQFP Package of AP918

5. BLOCK DIAGRAM

The following diagram shows the system blocks embedded in AP918.

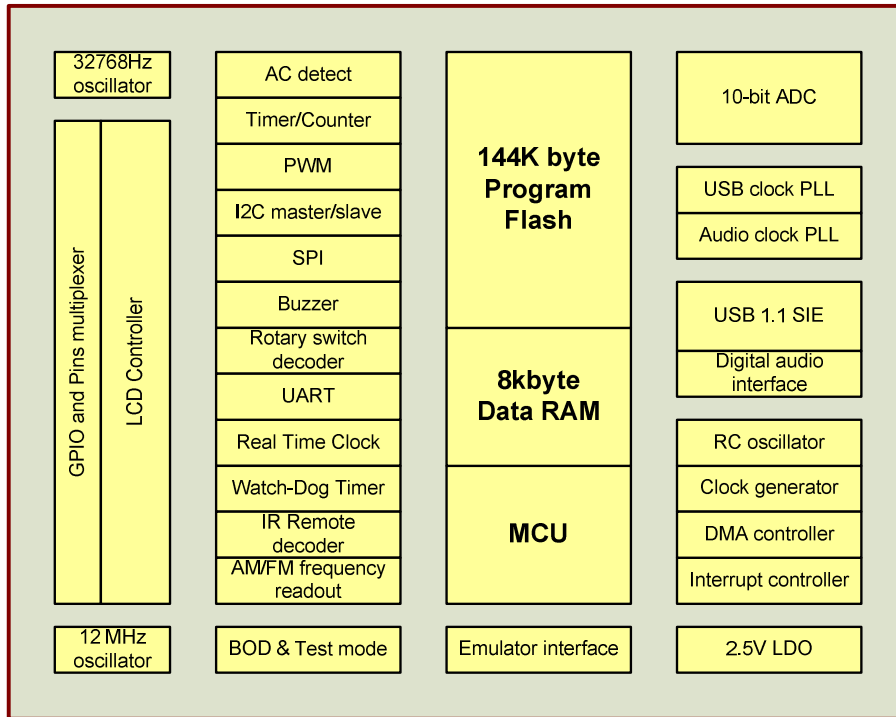


Figure 2 Internal Block Diagram of AP918

6. BUILT-IN PERIPHERALS

- 8-bit high performance, low power MCU
 - Operate at 32.768kHz up to 16MHz
 - Powerful instruction set : most single-cycle execution
 - 32 general purpose registers
 - Run, Stop and Power-down mode of operation
 - C or assembly programming
 - Serial emulator interface
 - Nonvolatile Program and Data Memories
 - 144K bytes of In-system reprogrammable Flash
 - Endurance: 20,000 cycles (min)
 - Page erase capability: 512 bytes per page
 - 8K bytes static data RAM
 - Peripheral Features
 - USB 2.0 Full Speed SIE
 - Host or Device mode operation
 - Supports bulk or isochronous transfer
 - 5 endpoints
 - 8 channels, 10-bit ADC
 - 8 channels
 - Automatic scanning and de-bouncing
 - Scan duty cycle control for power saving application
 - Clock generator
 - Software selectable MCU running frequency
 - Internal 8MHz RC oscillator with calibration features
 - 48 MHz PLL USB clock generator
 - Low jitter audio master clock generator PLL
 - Configurable 2 - 6 commons, 40 segments LCD interface
 - 96kHz 24 bit digital audio interface
 - Supports 4 stereo output and 1 stereo input
 - I2S, Left-justified or Right-justified interface
 - Master or slave mode
 - Real time clock counter with alarm interrupt and 32.768kHz reference clock calibration feature
 - 16-bit watch dog timer
 - Programmable frequency buzzer output
 - 50/60Hz AC line frequency detection
 - Dual programmable UART with 32 bytes transmit and receive FIFO
 - Three 12-bit PWM channels
 - Master mode SPI serial interface
 - One Master/Slave mode I2C interface
 - Three Master mode I2C interface
 - Dual 16-bit programmable timer/counter
 - 8-bit auto reload
 - Each can be configured as two 8-bit counters
 - One 16-bit programmable timer/counter with 16-bit auto reload and capture feature
 - IR remote signal decoder
 - NEC/Toshiba format
 - Pulse width counter to supports other remote format
 - Dual rotary switch counters with edge-detection for system wake-up
 - Digital frequency readout
 - AM and FM frequency range in BCD format
 - Data change interrupt
 - 83 GPIO pins
 - 1 external interrupt input pins
- Others
 - Power-on reset and Brown-out detection
 - On-chip 2.5V LDO regulator
 - 3.3V supply voltage
 - 100 LQFP

7. PIN DESCRIPTION

QFP 100	Name	Type	RS	Descriptions
1	ADC0/P10[0]	IO,S	Z	GPIO pin. ADC input.
2	ADC1/P10[1]	IO,S	Z	GPIO pin. ADC input.
3	ADC2/P10[2]	IO,S	Z	GPIO pin. ADC input.
4	ADC3/P10[3]	IO,S	Z	GPIO pin. ADC input.
5	ADC4/P10[4]	IO,S	Z	GPIO pin. ADC input.
6	ADC5/P10[5]	IO,S	Z	GPIO pin. ADC input.
7	ADC6/P10[6]	IO,S	Z	GPIO pin. ADC input.
8	ADC7/P10[7]	IO,S	Z	GPIO pin. ADC input.
9	TESTB	I,S	I	Active low test mode enabled input with internal pull-up.
10	PLLFLT2	IOA	Z	Audio clock PLL external filter connection pin.
11	AVCC	-	-	3.3V PLL supply voltage.
12	AGND	-	-	PLL analog ground.
13	RCK1/IRQ/P7[4]	IO,S	Z	Interrupt input. GPIO pin. Rotary switch encoder input.
14	RCD1/ P7[5]	IO,S	Z	GPIO pin. Rotary switch encoder input.
15	RCD0/ P7[6]	IO,S	Z	GPIO pin. Rotary switch encoder input.
16	RCK0 /P7[7]	IO,S	Z	GPIO pin. Rotary switch encoder input.
17	VLCD/P8[4]	IO,S	Z	GPIO pin. LCD bias.
18	V2/P9[7]	IO,S	Z	GPIO pin. LCD bias.
19	V1/P9[6]	IO,S	Z	GPIO pin. LCD bias.
20	COM6/I2CSCL1/P9[5]	IO,S	Z	GPIO pin. I2C interface clock. LCD common.
21	COM5/I2CSDA1/P9[4]	IO,S	Z	GPIO pin. I2C interface serial data.
22	DFR_FMIN/P8[3]	IO,S	Z	GPIO pin. Digital frequency FM input.
23	RSTB	I,S	I	Active low reset input.
24	DFR_AMIN/P8[2]	IO,S	Z	GPIO pin. Digital frequency AM input.
25	I2CSCL0/P8[1]	IO,S	Z	GPIO pin. I2C interface clock.
26	I2CSDA0/P8[0]	IO,S	Z	GPIO pin. I2C interface serial data.
27	COM4/LCDD7/P9[3]	IO,S	Z	GPIO pin. External LCD module interface data. LCD common.
28	COM3/LCDD6/P9[2]	IO,S	Z	GPIO pin. External LCD module interface data. LCD common.
29	COM2/LCDD5/P9[1]	IO,S	Z	GPIO pin. External LCD module interface data. LCD common.
30	COM1/LCDD4/P9[0]	IO,S	Z	GPIO pin. External LCD module interface data. LCD common.
31	SEG1/P0[0]	IO,S	Z	GPIO pin. LCD segment.
32	SEG2/P0[1]	IO,S	Z	GPIO pin. LCD segment.
33	SEG3/P0[2]	IO,S	Z	GPIO pin. LCD segment.
34	SEG4/P0[3]	IO,S	Z	GPIO pin. LCD segment.
35	SEG5/P0[4]	IO,S	Z	GPIO pin. LCD segment.
36	XI12M	I	I	12MHz oscillator input
37	XO12M	O	O	12MHz oscillator output
38	GND	-	-	System ground
39	VCC	-	-	3.3V power supply
40	VDD	-	-	On-chip LDO 2.5V output
41	REGPD	I	I	Active low LDO enable
42	SEG6/LCDRDX/P0[5]	IO,S	Z	GPIO pin. External LCD module interface read. LCD segment.
43	SEG7/LCDWRX/P0[6]	IO,S	Z	GPIO pin. External LCD module interface write. LCD segment.
44	SEG8/P0[7]	IO,S	Z	GPIO pin. LCD segment.
45	SEG9/P1[0]	IO,S	Z	GPIO pin. LCD segment.
46	SEG10/P1[1]	IO,S	Z	GPIO pin. LCD segment.
47	SEG11/P1[2]	IO,S	Z	GPIO pin. LCD segment.
48	SEG12/LCDA0/P1[3]	IO,S	Z	GPIO pin. External LCD module interface address. LCD segment.
49	SEG13/LCDD3/P1[4]	IO,S	Z	GPIO pin. External LCD module interface data. LCD segment.
50	SEG14/LCDD2/P1[5]	IO,S	Z	GPIO pin. External LCD module interface data. LCD segment.
51	SEG15/LCDD1/P1[6]	IO,S	Z	GPIO pin. External LCD module interface data. LCD segment.
52	SEG16/LCDD0/P1[7]	IO,S	Z	GPIO pin. External LCD module interface data. LCD segment.
53	SEG17/EMU_SCLR/P2[0]	IO,S	Z	GPIO pin. Emulator interface clear. LCD segment.
54	SEG18/EMU_SCLK/P2[1]	IO,S	PU	GPIO pin. Emulator interface clock. LCD segment. Default with internal pull-up enabled.
55	SEG19/EMU_SDI/P2[2]	IO,S	Z	GPIO. Emulator interface data input. LCD segment.
56	SEG20/EMU_SDO/P2[3]	IO,S	Z	GPIO. Emulator interface data output. LCD segment.
57	SEG21/P2[4]	IO,S	Z	GPIO pin. LCD segment.
58	SEG22/P2[5]	IO,S	Z	GPIO pin. LCD segment.
59	SEG23/P2[6]	IO,S	Z	GPIO pin. LCD segment.
60	SEG24/P2[7]	IO,S	Z	GPIO pin. LCD segment.
61	DP/P8[5]	IO,S	Z	GPIO. USB transceiver D+ pin
62	DM/P8[6]	IO,S	Z	GPIO. USB transceiver D- pin

QFP 100	Name	Type	RS	Descriptions
63	VCC	-	-	3.3V power supply
64	GND	-	-	System ground
65	XO32K	O	O	32768Hz oscillator output
66	XI32K	I	I	32768Hz oscillator input
67	SEG25/SPICSB/P3[0]	IO,S	Z	GPIO pin. SPI interface chip select. LCD segment.
68	SEG26/SPICLK/P3[1]	IO,S	Z	GPIO pin. SPI interface clock. LCD segment.
69	SEG27/SPISDO/P3[2]	IO	Z	GPIO pin. SPI interface data output. LCD segment.
70	SEG28/SPISDI/P3[3]	IO,S	Z	GPIO pin. SPI interface data input. LCD segment.
71	SEG29/UCLK1/P3[4]	IO,S	Z	GPIO pin. UART 16x baud clock. LCD segment.
72	SEG30/PWM0/P3[5]	IO,S	Z	GPIO. PWM output. LCD segment.
73	SEG31/PWM1/P3[6]	IO,S	Z	GPIO. PWM output. LCD segment.
74	SEG32/PWM2/P3[7]	IO,S	Z	GPIO. PWM output. LCD segment.
75	SEG33/I2CSCL3/ P4[0]	IO,S	Z	GPIO. I2C interface clock. LCD segment.
76	SEG34/I2CSDA3//P4[1]	IO,S	Z	GPIO. I2C interface clock. LCD segment.
77	SEG35/I2CSCL2/ P4[2]	IO,S	Z	GPIO pin. I2C interface clock. LCD segment.
78	SEG36/I2CSDA2/ P4[3]	IO,S	Z	GPIO pin. I2C interface clock. LCD segment.
79	SEG37/LCDCSX/UCLK0/P4[4]	IO,S	Z	GPIO. External LCD module chip select. UART 16x baud clock. LCD segment.
80	SEG38/BUZ/P4[5]	IO,S	Z	GPIO pin. Buzzer output. LCD segment.
81	SEG39/RX1/P5[4]	IO,S	Z	GPIO pin. UART receiver input.
82	SEG40/TX1/P5[5]	IO,S	Z	GPIO pin. UART transmitter output.
83	DAUDO2 /P6[0]	IO,S	Z	GPIO pin. Digital audio data output.
84	DAUDO3 /P6[1]	IO,S	Z	GPIO pin. Digital audio data output.
85	GND	-	-	System ground
86	VCC	-	-	3.3V power supply
87	MCLK	IO,S	Z	Digital audio master clock.
88	BCLK/ P6[3]	IO,S	Z	GPIO pin. Digital audio serial data clock.
89	LRCLK/ P6[4]	IO,S	Z	GPIO pin. Digital audio sampling frequency clock.
90	DAUDI/ P6[5]	IO,S	Z	GPIO pin. Digital audio data input.
91	DAUDO0/ P6[6]	IO,S	Z	GPIO pin. Digital audio data output.
92	DAUDO1/ P6[7]	IO,S	Z	GPIO pin. Digital audio data output.
93	EMU_SCLR/P7[0]	IO,S	Z	GPIO pin. Emulator interface clear.
94	EMU_SCLK/P7[1]	IO,S	PU	GPIO pin. Emulator interface clock. Default with internal pull-up enabled.
95	EMU_SDI/P7[2]	IO,S	Z	GPIO. Emulator interface data input.
96	EMU_SDO/P7[3]	IO,S	Z	GPIO. Emulator interface data output.
97	ACDET/P5[0]	IO,S	Z	GPIO pin. 50/60Hz ac frequency detection input.
98	REMO/P5[1]	IO,S	Z	GPIO pin. Remote decoder input.
99	RX0/P5[2]	IO,S	Z	GPIO pin. UART receiver input.
100	TX0/P5[3]	IO,S	Z	GPIO pin. UART transmitter output.

I - Input pin
 O - Output pin
 IO - Bidirectional pin
 IA - Analog input pin
 OA - Analog output pin

S - CMOS Schmitt Trigger
 (P)U - (Programmable) Pull-up
 (P)D - (Programmable) Pull-down
 L - LCD Pad
 0,1,Z - Logic state 0, Logic state 1, High impedance

8. ELECTRICAL SPECIFICATION

8.1. Absolute Maximum Rating

Item	Symbol	Rating	Unit
Power Supply Voltage (VCC)	VCC	-0.5 to 6.0	V
Analog Supply Voltage (AVCC)	AVCC	-0.5 to 6.0	V
Core Supply Voltage (VDD)	VDD	-0.5 to 6.0	V
Power Supply Voltage (LCD)	VLCD/V2/V1	-0.5 to 6.0	V
Input Voltage	V _{IN}	-0.5 to VCC+ 0.5	V
Power Dissipation (Ta = 70°C)	Pd	TBD	mW
Storage Temperature	T _{STG}	-20 to 125	°C
Operating Temperature	T _{OPR}	0 to 70	°C

8.2. Recommended Operating Condition

Item	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage (VCC)	VCC	3.0	3.3	3.6	V
Power supply voltage (AVCC)	AVCC	3.0	3.3	3.6	V
Power supply voltage (VDD)	VDD	2.25	2.5	2.75	V
Input voltage	V _{IN}	0	-	VCC	V
Input voltage (DFR_FMIN) 120MHz to 150MHz	V _{IN}	1	-	-	mV
Input voltage (DFR_AMIN) 12MHz to 30MHz	V _{IN}	5	-	-	mV
Operating temperature	T _{OPR}	0	-	70	°C

8.3. Leakage Current and Capacitance

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I _{IN}	Input current	No pull-up or pull-down	-10	-	10	μA
I _{OZ}	Tri-state leakage current		-10	-	10	μA
C _{IN}	Input pin capacitance			8		pF
C _{OUT}	Output pin capacitance			8		pF
C _{BID}	Bidirectional pin capacitance			8		pF

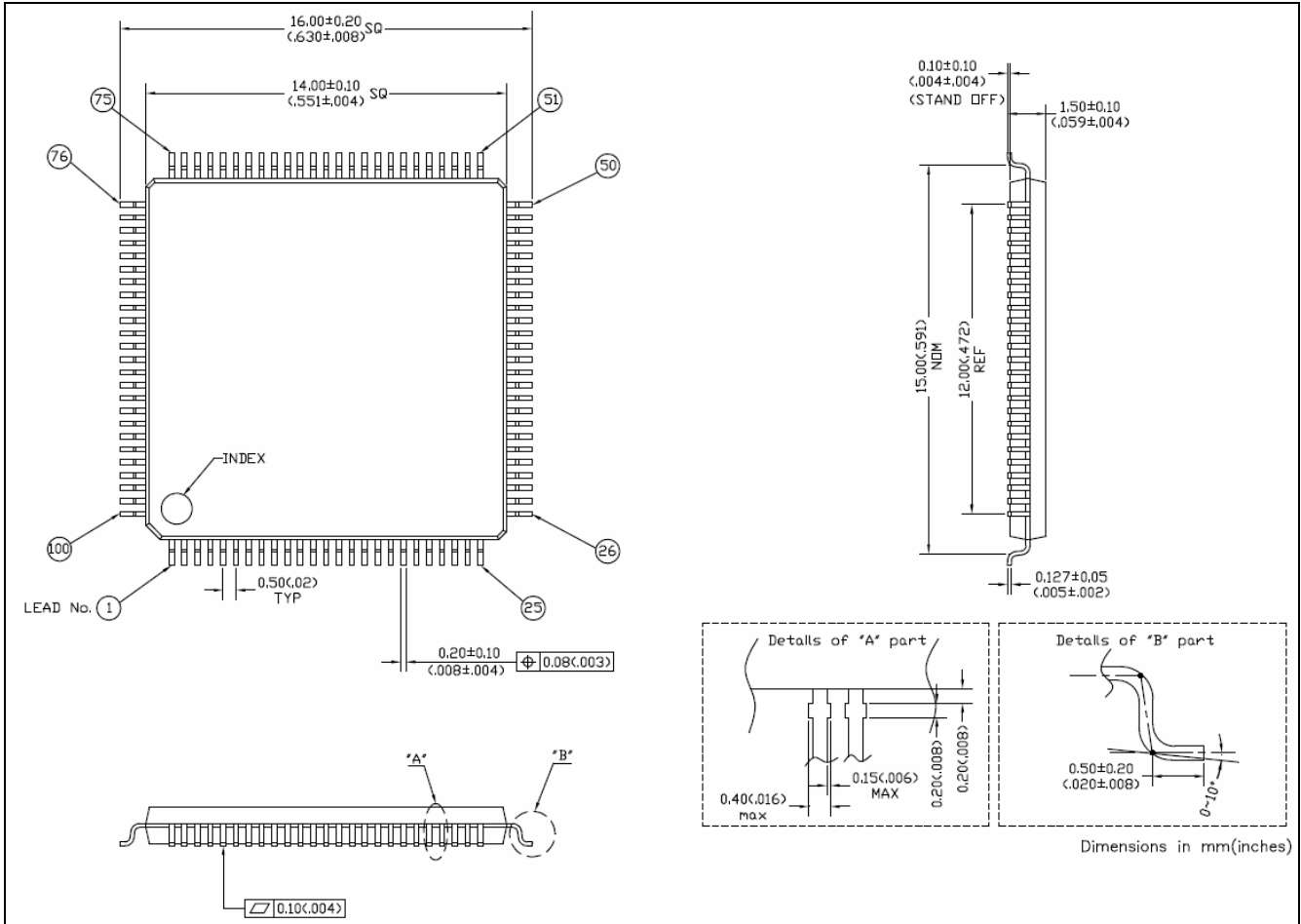
8.4. DC Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
GPIO buffer						
V _{IH1}	Input high voltage (All except MCLK pin)	-	0.6*VCC	-	-	V
V _{IL1}	Input low voltage (All except MCLK pin)	-	-	-	0.4*VCC	V
R _{PU}	Pull-up resistance GPIO and TESTB pins	V _{IN} = 0V	30	50	85	kΩ
R _{LBIASL}	LCD internal biasing resistor	Low biasing		330		kΩ
R _{LBIASH}	LCD internal biasing resistor	Strong biasing		31		kΩ
I _{OL1}	Output low current (All except MCLK pin)	V _{OL} = 0.4V	3	5		mA
I _{OH1}	Output high current (All except MCLK pin)	V _{OH} = VCC - 0.4V	3	4		mA
I _{OL2}	Output low current (MCLK pin)	V _{OL} = 0.4V	9	11		mA
I _{OH2}	Output high current (MCLK pin)	V _{OH} = VCC - 0.4V	7	9		mA
V _{IH2}	Input high voltage (MCLK pin)	-	0.54*VCC	-	-	V
V _{IL2}	Input low voltage (MCLK pin)	-	-	-	0.46*VCC	V
2.5V LDO						
V _{DD}	Output voltage	Load current = 35mA	2.4	2.5	2.6	V
V _{DROP}	Dropout voltage	Load current = 35mA <i>Note 1</i>			170	mV
ΔV _{DD}	Line Regulation	V _{CC} =2.75V to 3.6V			0.3	%
ΔV _{DD}	Load Regulation	Load current = 1mA to 35mA			0.3	mV/mA
10-bit ADC						
V _{IN}	Full scale input span		0		VCC	V
INL	Integral linearity error				±2	LSB
DNL	Differential linearity error				±0.75	LSB
V _{offset}	Input offset error				±2	mV
Current Consumption (sum of current draw at VCC and AVCC)						
I _{dd_opr}	Operating current	<i>Note 2</i>	-	25	-	mA
I _{dd_rtc}	Real time clock current	<i>Note 3</i>	-	50	80	μA
I _{dd_stdby}	Standby current	<i>Note 4</i>	-	30	40	μA

Note:

- 1 This is simulation data only.
- 2 No load on all pins, LDO enabled, MCU run at 12MHz, ADC enabled, PLL enabled.
- 3 No load on all pins, LDO enabled, CPU clock source use RCOSC, RTC running, ADC disabled, PLL disabled, USB suspend, 12MHz oscillator disabled, short flash read pulse enabled, use timer interrupt to wake up CPU.
- 4 All oscillator disabled, USB suspend, ADC disabled, PLL disabled, USB suspend, all GPIO pins output drive H

9. PACKAGE INFORMATION



10. SOLDERING INDICATION

This section gives a very brief insight to a complex technology. There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

1. Reflow Soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stenciling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250°C. The top-surface temperature of the packages should preferably be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

2. Wave Soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used, the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch:
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250°C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

3. Manual Soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

4. Suitability of Surface Mount IC Packages for Wave and Reflow Soldering Methods

Package	Soldering Method	
	Wave	Reflow ⁽¹⁾
BGA, HBGA, LFBGA, SQFP, TFBGA	Not suitable ⁽²⁾	Suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	Not suitable	Suitable
PLCC (3), SO, SOJ	Suitable	Suitable
LQFP, QFP, TQFP	Not recommended ⁽³⁾⁽⁴⁾	Suitable
SSOP, TSSOP, VSO	Not recommended ⁽⁵⁾	Suitable

Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect).
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch equal to or smaller than 0.5 mm.



Valence Semiconductor Design Limited
Unit 2001, 20/F, APEC Plaza,
49 Hoi Yuen Road, Kwun Tong, Hong Kong
Tel: (852) 2797 3288
Fax: (852) 2776 7770
Email: inquiry@valencetech.com
Website: <http://www.valencetech.com>

IMPORTANT NOTICE

"Preliminary" product information describes products that are in production, but for which full characterization data is not yet available. ValenceTech Ltd. and its affiliates ("Valence") believe that the information contained in this document is accurate and reliable. However, the information is subject to change without notice and is provided "AS IS" without warranty of any kind (express or implied). Customers are advised to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability. No responsibility is assumed by Valence for the use of this information, including use of this information as the basis for manufacture or sale of any items, or for infringement of patents or other rights of third parties. This document is the property of Valence and by furnishing this information, Valence grants no license, express or implied under any patents, mask work rights, copyrights, trademarks, trade secrets or other intellectual property rights. Valence owns the copyrights associated with the information contained herein and gives consent for copies to be made of the information only for use within your organization with respect to Valence integrated circuits or other products of Valence. This consent does not extend to other copying such as copying for general distribution, advertising or promotional purposes, or for creating any work for resale. An export permit needs to be obtained from the competent authorities of the Japanese Government if any of the products or technologies described in this material and controlled under the "Foreign Exchange and Foreign Trade Law" is to be exported or taken out of Japan. An export license and/or quota needs to be obtained from the competent authorities of the Chinese Government if any of the products or technologies described in this material is subject to the PRC Foreign Trade Law and is to be exported or taken out of the PRC. CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). VALENCE PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN AIRCRAFT SYSTEMS, MILITARY APPLICATIONS, PRODUCTS SURGICALLY IMPLANTED INTO THE BODY, LIFE SUPPORT PRODUCTS OR OTHER CRITICAL APPLICATIONS (INCLUDING MEDICAL DEVICES, AIRCRAFT SYSTEMS OR COMPONENTS AND PERSONAL OR AUTOMOTIVE SAFETY OR SECURITY DEVICES). INCLUSION OF VALENCE PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK AND VALENCE DISCLAIMS AND MAKES NO WARRANTY, EXPRESS, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR PARTICULAR PURPOSE, WITH REGARD TO ANY VALENCE PRODUCT THAT IS USED IN SUCH A MANNER. IF THE CUSTOMER OR CUSTOMER'S CUSTOMER USES OR PERMITS THE USE OF VALENCE PRODUCTS IN CRITICAL APPLICATIONS, CUSTOMER AGREES, BY SUCH USE, TO FULLY INDEMNIFY VALENCE, ITS OFFICERS, DIRECTORS, EMPLOYEES, DISTRIBUTORS AND OTHER AGENTS FROM ANY AND ALL LIABILITY, INCLUDING ATTORNEYS' FEES AND COSTS, THAT MAY RESULT FROM OR ARISE IN CONNECTION WITH THESE USES.