AP733

DIGITAL VOICE RECORDER CONTROLLER with Error Correction Code

Data Sheet

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1. OVERVIEW

The AP733 Digital Voice Recorder Controller is an ASIC chip for digitally recording and playing back of voice signals. It has built-in a 16-bit DSP for speech signal encoding and decoding. An 8-bit CPU is also built-in for handling user interface, USB protocol and memory management, etc. The built-in codec with automatic level control input also helps to minimize the external components to be used for building a microphone related product.

2. APPLICATION

2.1 Target Application

- Digital Voice Recorder

2.2 Application Features

2.2.1 Voice Interface

- Built-in operational amplifiers for microphone signal amplification and automatic level control used
- Sigma delta ADC for digitizing the voice signal
- Sigma delta DAC for converting the digital PCM data into analog voice signal

2.2.2 USB Interface

- Supports one USB bulk transfer capability
- Built-in USB SIE

2.2.3 DSP Core

- 16-bit DSP core

2.2.4 MCU Core

- 8-bit MCU core
- RISC architecture

2.2.5 Other Features

- I2C / 6800 / 8080 Interface for external LCD driver
- NAND / AND flash interface – build in ECC (Error correction Code)
- Secure Digital / Multimedia Card Interface
- USB interface
- Programmable I/O ports
- Built-in timers and counter
- Hardware real time clock

3. ORDERING INFORMATION

ORDERING NUMBER	PADS	PACKAGE
AP733-DC-L	117	DICE

4. SYSTEM BLOCK DIAGRAM

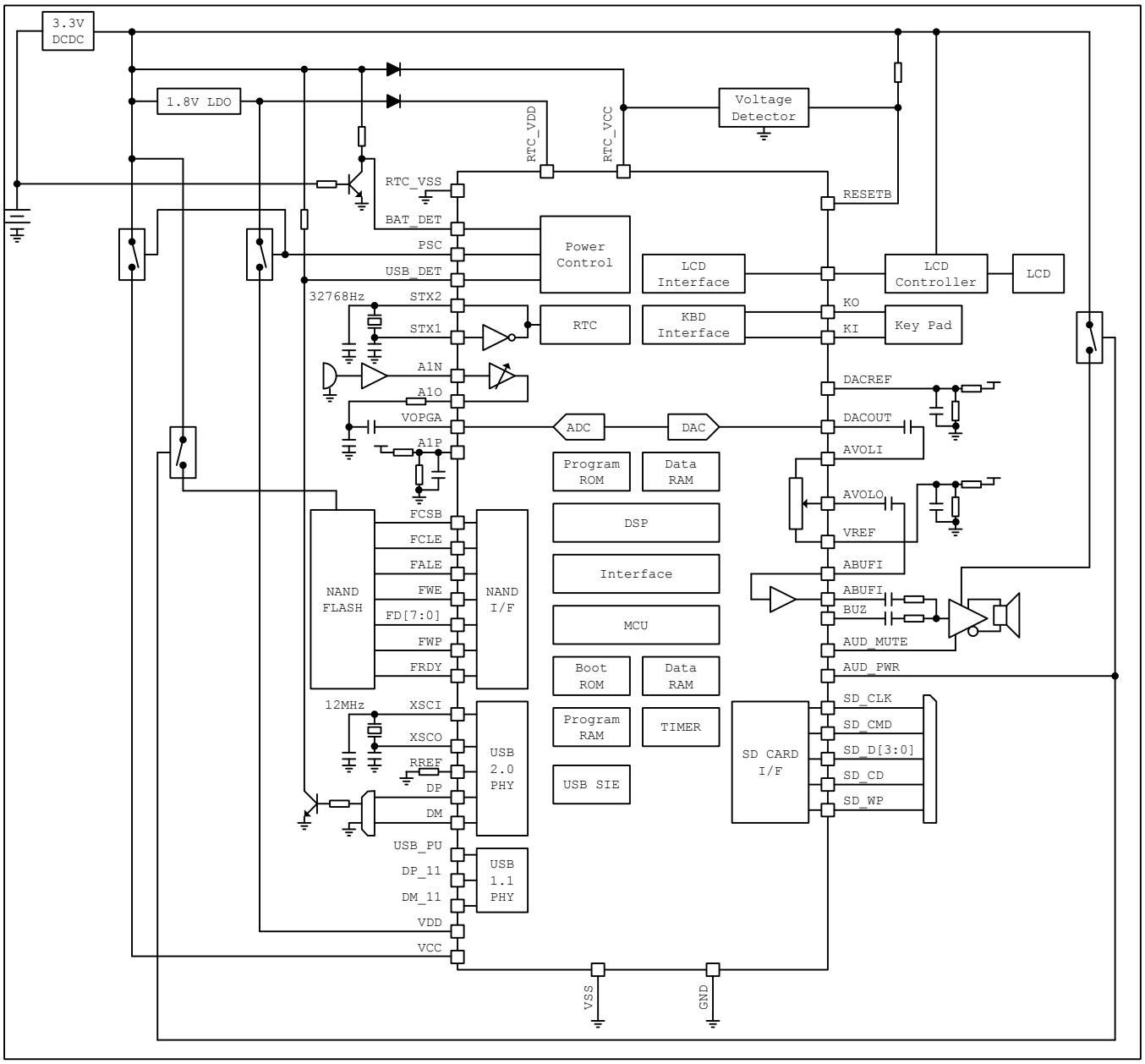

Figure 1 Block Diagram of Digital Voice Recorder Controller

5. DEVICE PIN DESCRIPTION

Pad No	NAME	DESCRIPTION
1	LCDD[6]	D6 of 6800 / 8080 Interface / I2C Data
2	LCDD[5]	D5 of 6800 / 8080 Interface
3	LCDD[4]	D4 of 6800 / 8080 Interface
4	RTCVCC	3.3V I/O Power of RTC
5	RTCVSS	I/O Ground of RTC
6	LCDD[3]	D3 of 6800 / 8080 Interface
7	LCDD[2]	D2 of 6800 / 8080 Interface
8	LCDD[1]	D4 of 6800 / 8080 Interface
9	LCDD[0]	D4 of 6800 / 8080 Interface
10	LCDCSB	Chip Select Signal of 6800 / 8080 Interface
11	KO[4]	Key Matrix Scan Output Bit 4
12	KO[3]	Key Matrix Scan Output Bit 3
13	LCDRW	Read / Write Signal of 6800 Interface / Write Signal of 8080 Interface
14	LCDE	Strobe Signal of 6800 Interface / Read Signal of 8080 Interface
15	TEST1B	Test Signal for IC Test, Open for Normal Operation
16	TEST2B	Test Signal for IC Test, Open for Normal Operation
17	RESETB	System Reset, Active Low
18	RTCVDD	1.8V Core Power of RTC
19	GND	Core Ground
20	SXT1	32768Hz Oscillator Input
21	SXT2	32768Hz Oscillator Output
22	RTCVCC	3.3V I/O Power of RTC
23	RTCVSS	I/O Ground of RTC
24	KO[0]	Key Matrix Scan Output Bit 0
25	KO[1]	Key Matrix Scan Output Bit 1
26	KO[2]	Key Matrix Scan Output Bit 2
27	KI[0]	Key Matrix Scan Input Bit 0
28	KI[1]	Key Matrix Scan Input Bit 1
29	KI[2]	Key Matrix Scan Input Bit 2
30	KI[3]	Key Matrix Scan Input Bit 3
31	PSC	Power Control, Active High
32	BAT_DET	Battery Detect, Active Low
33	USB_DET	USB Detect, Active Low
34	VDD	1.8V Core Power
35	GND	Core Ground
36	XSCI	12MHz Oscillator Input
37	XSCO	12MHz Oscillator Output
38	VCC	3.3V Analog Power of USB 2.0 PHY
39	VDD	1.8V Analog Power of USB 2.0 PLL
40	DM	DM of USB 2.0
41	DP	DP of USB 2.0
42	VSS	Analog Ground of USB 2.0 PHY
43	RREF	Reference of USB 2.0 PHY, Connect 12K 1% Resistor to Ground
44	GND	Analog Ground of USB 2.0 PLL

45	VDD	1.8V Core Power
46	GND	Core Ground
47	DSDO	Debugger Serial Data Output
48	VSS	I/O Ground
49	VCC	3.3V I/O Supply
50	DCLR	Debugger Clear Signal
51	DCLK	Debugger Serial Clock Input
52	DSDI	Debugger Serial Data Input
53	ADC[0]	6 bit ADC Channel 0
54	ADC[1]	6 bit ADC Channel 1
55	ADC[2]	6 bit ADC Channel 2 / SPI Serial Data In
56	ADC[3]	6 bit ADC Channel 3 / SPI Serial Data Out
57	LED0	LED Output 0 / SPI Chip Select
58	LED1	LED Output 1 / SPI Serial Clock
59	FD[3]	NAND FLASH Data Bit 3
60	FD[2]	NAND FLASH Data Bit 2
61	FD[1]	NAND FLASH Data Bit 1
62	FD[0]	NAND FLASH Data Bit 0
63	FWP	NAND FLASH Write Protect
64	FWE	NAND FLASH Write Strobe
65	VCC	3.3V I/O Power
66	VSS	I/O Ground
67	SD_WP	PWM / SD Card Write Protect
68	SD_CD	SD Card Detect
69	VDD	1.8V Core Power
70	GND	Core Ground
71	SD_D[1]	SD Card Serial Data Bit 1
72	SD_D[0]	SD Card Serial Data Bit 0
73	SD_CLK	SD Card Serial Clock
74	SD_CMD	SD Card Serial Command
75	SD_D[3]	SD Card Serial Data Bit 3
76	SD_D[2]	SD Card Serial Data Bit 2
77	VCC	3.3V I/O Power
78	VSS	I/O Ground
79	FALE	NAND FLASH Address Latch Enable
80	FCLE	NAND FLASH Command Latch Enable
81	FCSB	NAND FLASH Chip Select
82	FRE	NAND FLASH Read Strobe
83	FRDY	NAND FLASH Ready Signal
84	FD[7]	NAND FLASH Data Bit 7
85	FD[6]	NAND FLASH Data Bit 6
86	FD[5]	NAND FLASH Data Bit 5
87	FD[4]	NAND FLASH Data Bit 4
88	AUD_PWR	Audio Power, Active Low
89	AUD_MUTE	Audio Mute
90	VCC	3.3V I/O Power
91	VSS	I/O Ground

92	BUZ	Buzzer Output
93	VDD	1.8V Core Power
94	GND	Core Ground
95	AGND	Analog Core Ground
96	PFIL	PLL Filter
97	AVDD	1.8V Analog Power
98	ATEST4	Analog Test 4 for IC Test, Open for Normal Operation
99	SPKOUT	Audio Output to Power Amp.
100	ABUFI	Audio Buffer Input
101	AVOLO	Audio Volume Output
102	AVOLI	Audio Volume Input
103	AVSS	Analog I/O Ground
104	VREF	Reference Voltage of Volume Control
105	DACREF	Reference Voltage of Audio DAC
106	DACOUT	Audio DAC Output
107	AVCC	3.3V Analog I/O Power
108	ATEST3	Analog Test 3 for IC Test, Open for Normal Operation
109	ATEST2	Analog Test 2 for IC Test, Open for Normal Operation
110	ATEST1	Analog Test 1 for IC Test, Open for Normal Operation
111	ATEST0	Analog Test 0 for IC Test, Open for Normal Operation
112	VOPGA	Audio ADC Input
113	A1O	Audio Op-amp Output
114	A1P	Audio Op-amp Non-inverting Input
115	A1N	Audio Op-amp Inverting Input
116	LCDRS	6800 / 8080 Interface Command / Data Select
117	LCDD[7]	D7 of 6800 / 8080 Interface / I2C Clock

6. ELECTRICAL SPECIFICATION

6.1 Absolute Maximum Ratings

Under no circumstances the absolute maximum ratings given below should be violated. Stresses exceeding one or more of the limiting values may cause permanent damage to the device.

Parameter	Symbol	Rating	Unit
Power Supply Voltage (I/O)	VCC	-0.5 to 7.0	V
Power Supply Voltage (Core)	VDD	TBD	V
Power Supply Voltage (Analog I/O)	AVCC	-0.5 to 7.0	V
Power Supply Voltage (Analog Core)	AVDD	TBD	V
Input Voltage	Vin	-0.5 to VDD+0.5	V
Power Dissipation (Ta = 70°C)	Pd	100	mW
Storage Temperature	Tstg	-20 to 125	°C
Operating Temperature	Topr	0 to 70	°C

6.2 Recommended Operating Condition

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage (I/O)	VCC	3.0	-	3.6	V
Power Supply Voltage (Core)	VDD	1.7	-	1.9	V
Power Supply Voltage (Analog I/O)	AVCC	3.0	-	3.6	V
Power Supply Voltage (Analog Core)	AVDD	1.7	-	1.9	V
Input Voltage (digital)	Vin	0	-	VCC	V
Input Voltage (analog)	Vin	0	-	VCC	V
Operating Temperature	Topr	0	-	70	°C

6.3 Electrical Characteristics

(VDD=3.3V±10%, AVDD=3.3V±5%, Operating temperature = 0°C - 70°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply Voltage (logic)		3.0	-	3.6	V
AVDD	Supply Voltage (analog)		3.0	-	3.6	V
V_{IH}	Input high voltage		$0.8V_{DD}$	-	-	V
V_{IL}	Input low voltage		-	-	$0.2V_{DD}$	V
V_{IHS}	Schmitt Trigger Input High voltage		$0.7V_{DD}$	-	-	V
V_{ILS}	Schmitt Trigger Input low voltage		-	-	$0.3V_{DD}$	V
V_{THS}	Schmitt Trigger Input Threshold		$0.4\ V_{DD}$	-	-	V
I_{OL}	Output Low Current	VOL = 1.5V	-	4	-	mA
I_{OH}	Output High Current	VOH = VCC – 0.4V	-	4	-	mA

7. BONDING DIAGRAM

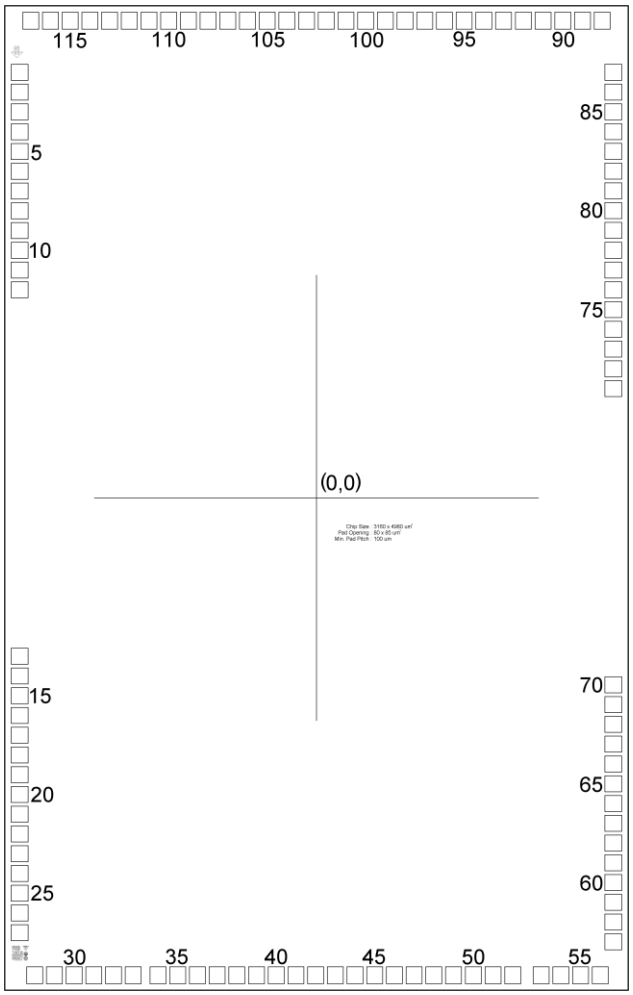

Figure 2 Chip Information

Die Size : 3160 x 4980 um^2
Substrate : Connect to GND
Pad Opening : 80 x 85 um^2
Min. Pad Pitch : 100 um
Co-ordinate (0,0) located at center of die.

Pad No	NAME	COORDINATE	
		X	Y
1	LCDD[6]	-1507.00	2154.80
2	LCDD[5]	-1507.00	2054.80
3	LCDD[4]	-1507.00	1954.80
4	RTCVCC	-1507.00	1854.50
5	RTCVSS	-1507.00	1754.50
6	LCDD[3]	-1507.00	1654.20
7	LCDD[2]	-1507.00	1554.20
8	LCDD[1]	-1507.00	1454.20
9	LCDD[0]	-1507.00	1354.20
10	LCDCSB	-1507.00	1254.20
11	KO[4]	-1507.00	1154.20
12	KO[3]	-1507.00	1054.20
13	LCDRW	-1507.00	-800.88
14	LCDE	-1507.00	-900.88
15	TEST1B	-1507.00	-1000.88
16	TEST2B	-1507.00	-1100.88
17	RESETB	-1507.00	-1200.88
18	RTCVDD	-1507.00	-1301.18
19	GND	-1507.00	-1401.18
20	SXT1	-1507.00	-1501.18
21	SXT2	-1507.00	-1601.18
22	RTCVCC	-1507.00	-1701.18
23	RTCVSS	-1507.00	-1801.18
24	KO[0]	-1507.00	-1901.48
25	KO[1]	-1507.00	-2001.48
26	KO[2]	-1507.00	-2101.48
27	KI[0]	-1507.00	-2201.48
28	KI[1]	-1431.21	-2417.00
29	KI[2]	-1331.21	-2417.00
30	KI[3]	-1231.21	-2417.00
31	PSC	-1131.21	-2417.00
32	BAT_DET	-1031.21	-2417.00
33	USB_DET	-931.21	-2417.00
34	VDD	-805.06	-2417.00
35	GND	-705.06	-2417.00
36	XSCI	-605.06	-2417.00
37	XSCO	-505.06	-2417.00
38	VCC	-405.06	-2417.00
39	VDD	-305.06	-2417.00
40	DM	-205.06	-2417.00
41	DP	-105.06	-2417.00
42	VSS	-5.06	-2417.00
43	RREF	94.94	-2417.00
44	GND	194.94	-2417.00

45	VDD	294.94	-2417.00
46	GND	394.94	-2417.00
47	DSDO	495.24	-2417.00
48	VSS	595.54	-2417.00
49	VCC	695.54	-2417.00
50	DCLR	795.84	-2417.00
51	DCLK	895.84	-2417.00
52	DSDI	995.84	-2417.00
53	ADC[0]	1140.46	-2417.00
54	ADC[1]	1240.46	-2417.00
55	ADC[2]	1340.46	-2417.00
56	ADC[3]	1440.46	-2417.00
57	LED0	1507.00	-2247.00
58	LED1	1507.00	-2147.00
59	FD[3]	1507.00	-2047.00
60	FD[2]	1507.00	-1947.00
61	FD[1]	1507.00	-1847.00
62	FD[0]	1507.00	-1747.00
63	FWP	1507.00	-1647.00
64	FWE	1507.00	-1547.00
65	VCC	1507.00	-1446.70
66	VSS	1507.00	-1346.70
67	SD_WP	1507.00	-1246.40
68	SD_CD	1507.00	-1146.40
69	VDD	1507.00	-1046.10
70	GND	1507.00	-946.10
71	SD_D[1]	1507.00	554.20
72	SD_D[0]	1507.00	654.20
73	SD_CLK	1507.00	754.20
74	SD_CMD	1507.00	854.20
75	SD_D[3]	1507.00	954.20
76	SD_D[2]	1507.00	1054.20
77	VCC	1507.00	1154.50
78	VSS	1507.00	1254.50
79	FALE	1507.00	1354.80
80	FCLE	1507.00	1454.80
81	FCSB	1507.00	1554.80
82	FRE	1507.00	1654.80
83	FRDY	1507.00	1754.80
84	FD[7]	1507.00	1854.80
85	FD[6]	1507.00	1954.80
86	FD[5]	1507.00	2054.80
87	FD[4]	1507.00	2154.80
88	AUD_PWR	1450.45	2417.00
89	AUD_MUTE	1350.45	2417.00
90	VCC	1250.15	2417.00
91	VSS	1150.15	2417.00

92	BUZ	1049.85	2417.00
93	VDD	949.55	2417.00
94	GND	849.55	2417.00
95	AGND	749.55	2417.00
96	PFIL	649.55	2417.00
97	AVDD	549.55	2417.00
98	ATEST4	449.55	2417.00
99	SPKOUT	349.55	2417.00
100	ABUFI	249.55	2417.00
101	AVOLO	149.55	2417.00
102	AVOLI	49.55	2417.00
103	AVSS	-50.45	2417.00
104	VREF	-150.45	2417.00
105	DACREF	-250.45	2417.00
106	DACOUT	-350.45	2417.00
107	AVCC	-450.45	2417.00
108	ATEST3	-550.45	2417.00
109	ATEST2	-650.45	2417.00
110	ATEST1	-750.45	2417.00
111	ATEST0	-850.45	2417.00
112	VOPGA	-950.45	2417.00
113	A1O	-1050.45	2417.00
114	A1P	-1150.45	2417.00
115	A1N	-1250.45	2417.00
116	LCDRS	-1350.45	2417.00
117	LCDD[7]	-1450.45	2417.00

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