AP707

Flash Microcontroller for Hi-Fi System Application

Datasheet

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1. OVERVIEW

The AP707 is a powerful dedicated system-on-a-chip (SOC) for audio and Hi-Fi applications. With a powerful MCU, DSP and the USB interface, the AP707 is a complete single chip low-power audio decoder. The AP707 system is capable of playback MP3 on USB disk or SD card, digital audio streaming from the PC or iPOD. Application includes BlueTooth speaker, digital audio iPOD docking station, PC USB audio.

2. APPLICATIONS

2.1. Target Applications

- Docking system
- BlueTooth speaker
- USB audio streaming supports up to 96kHz 24bit stereo audio

2.2. Application Features

2.2.1 USB Audio Feature

- Playback audio file from iPhone/iPod/iPad through USB interface or PC USB audio streaming

2.2.2 Audio decoding

- MP3/SBC

2.2.2 Docking Control Features

- Docking control through front panel buttons or remote controller
- Device charging through docking system
- Support Apple Authentication Coprocessor

2.2.3 Clock and Alarm Features

- 12/24 hour clock display mode selectable by user
- Dual alarm clocks
- User selectable alarm mode – wake-to-buzzer, wake-to-radio or wake-to-docked device
- Fixed snooze feature
- Programmable sleep timer

2.2.5 Other System Features

- Low standby current
- 0℃ to 80℃ Operating temperature range
- Firmware upgrade

3. ORDERING INFORMATION

ORDERING NUMBER	PINS	PACKAGE
AP707-LQ-L	64	LQFP

4. PIN CONFIGURATION

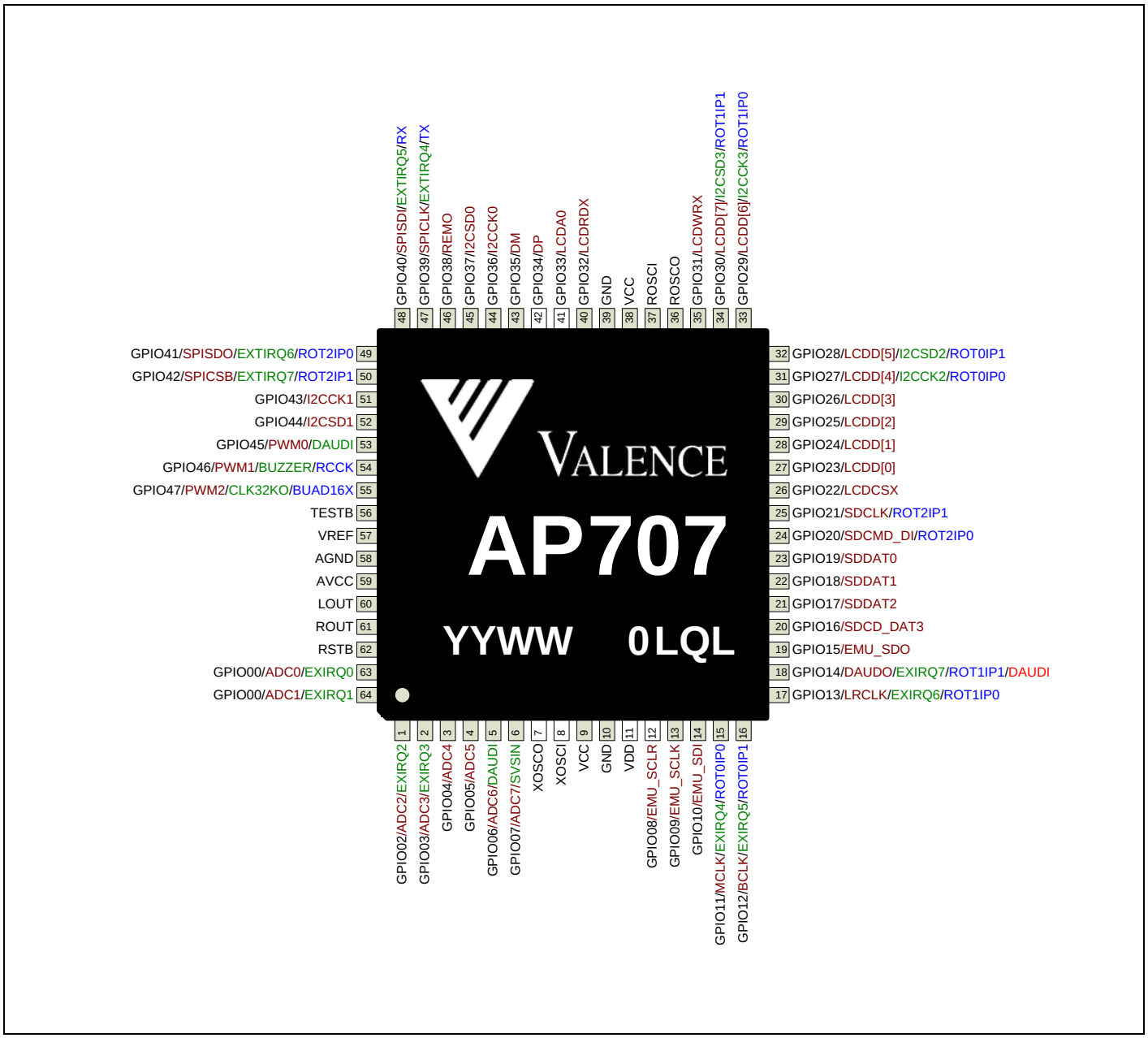


Figure 4-1 64-Pin LQFP Package of AP707

5. BLOCK DIAGRAM

The following diagram shows the system blocks embedded in AP707.

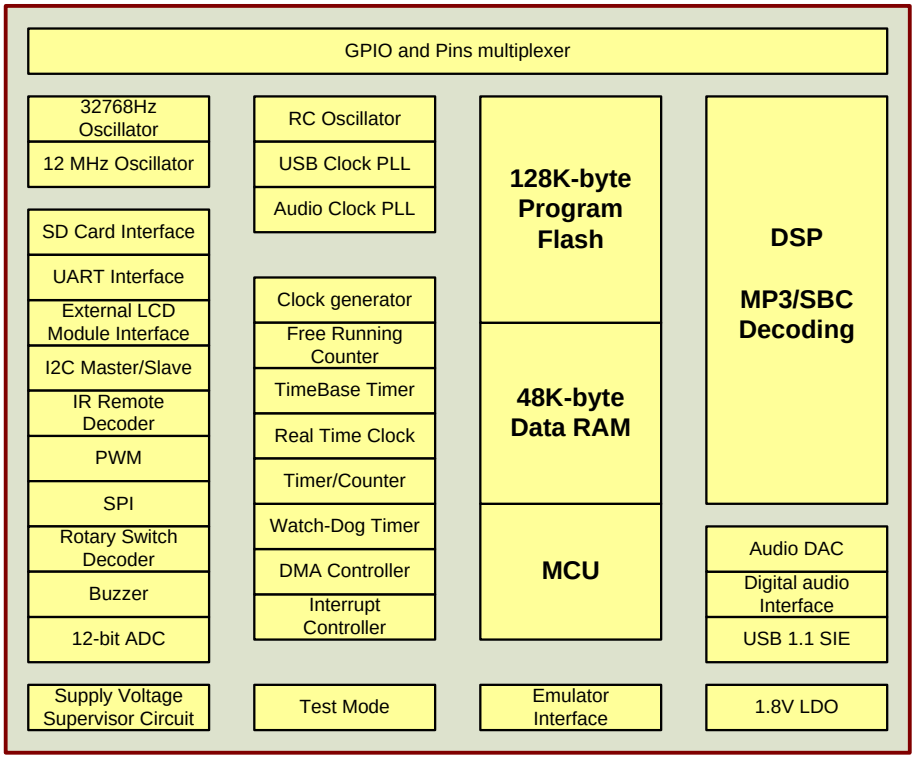


Figure 5-1 Internal Block Diagram of AP707

6. BUILT-IN PERIPHERALS

- 8-bit high performance, low power MCU
  - Operate at 32.768kHz up to 12MHz
  - Powerful instruction set : most single-cycle execution
  - 32 general purpose registers
  - Run, Stop and Power-down mode of operation
  - C or assembly programming
  - Serial emulator interface

- Nonvolatile Program and Data Memories
  - 128K bytes of In-system Flash
    - Endurance: 10,000 cycles (min)
    - Data retention: 10 years (min)
  - 48K bytes static data RAM

- 24-bit high performance, low power DSP
  - MP3/SBC decoding

- Peripheral Features
  - USB 2.0 Full Speed SIE
    - Host or Device mode operation
    - Supports bulk or isochronous transfer
    - 12 endpoints
  - 8 channels, 10-bit ADC
    - 8 channels
    - Automatic scanning and de-bouncing
    - Scan duty cycle control for power saving application
  - Clock generator
    - Software selectable MCU running frequency
    - Internal spread spectrum 8MHz RC oscillator with calibration features
    - 48 MHz PLL USB clock generator
    - Low jitter audio master clock generator PLL
  - 12-bit SAR ADC
  - SD card interface
  - 96kHz 24 bit audio digital audio interface
    - Supports 1 stereo output and 1 stereo input
    - I2S, Left-justified or Right-justified interface
    - Master or slave mode
  - Real time clock counter with alarm interrupt and 32.768kHz reference clock calibration feature
  - Programmable UART with 4k bytes transmit and receive FIFO
    - Supports up to 4 Mbps
  - 6800/8080 interface for external LCD module connection
  - 16-bit watch dog timer
  - Programmable frequency buzzer output
  - Three 12-bit PWM channels
  - Master/slave mode SPI serial interface
  - Four Master/Slave mode I2C interface
  - Dual 16-bit programmable timer/counter
    - 8-bit auto reload
    - Each can be configured as two 8-bit counters
  - One 16-bit programmable timer/counter with 16-bit auto reload and capture feature
  - IR remote signal decoder
    - NEC/Toshiba format
    - Pulse width counter to supports other remote format
  - Dual rotary switch counters with edge-detection for system wake-up
  - 48 GPIO pins
  - 8 external interrupt input pins

- Others
  - Power-on reset and Brown-out detection
  - On-chip 1.8V LDO regulator
  - 3.3V supply voltage
  - 0.18um CMOS process
  - 64 LQFP

7. PIN DESCRIPTION

LQFP64	Name	Type	RS	Descriptions
1	GPIO02/ADC2/EXIRQ2	IO,S	Z	GPIO pin, ADC input or external interrupt input
2	GPIO03/ADC3/EXIRQ3	IO,S	Z	GPIO pin, ADC input or external interrupt input
3	GPIO04/ADC4	IO,S	Z	GPIO pin or ADC input
4	GPIO05/ADC5	IO,S	Z	GPIO pin or ADC input
5	GPIO06/ADC6/DAUDI	IO,S	I	GPIO pin, ADC input or digital audio input
6	GPIO07/ADC7/SVSIN	IO,S	Z	GPIO pin, ADC input or supply voltage supervisor (SVS) input
7	XOSCO	O	O	12MHz oscillator output
8	XOSCI	I	I	12MHz oscillator input
9	VCC	-	-	3.3V power supply
10	GND	-	-	System ground
11	VDD	-	-	On-chip LDO 1.8V output
12	GPIO08/EMU_SCLR	IO,S	Z	GPIO pin or MCU emulator interface clear input
13	GPIO09/EMU_SCLK	IO,S	Z	GPIO pin or MCU emulator interface clock input
14	GPIO10/EMU_SDI	IO,S	Z	GPIO pin or MCU emulator interface serial data input
15	GPIO11/MCLK/EXIRQ4/ROT0IP0	IO,S	Z	GPIO pin, digital audio interface master clock, external interrupt or rotary switch decoder input
16	GPIO12/BCLK/EXIRQ5/ROT0IP1	IO,S	Z	GPIO pin, digital audio interface serial bit clock, external interrupt or rotary switch decoder input
17	GPIO13/LRCLK/EXIRQ6/ROT1IP0	IO,S	Z	GPIO pin, digital audio interface sampling clock, external interrupt or rotary switch decoder input
18	GPIO14/DAUDO/EXIRQ7/ROT1IP1/DAUDI	IO,S	Z	GPIO pin, digital audio interface data output, external interrupt, rotary switch decoder input or digital audio interface data input.
19	GPIO15/EMU_SDO	IO,S	Z	GPIO pin or MCU emulator interface serial data output
20	GPIO16/SDCD_DAT3	IO,S	Z	GPIO pin or SD card interface data bus
21	GPIO17/SDDAT2	IO,S	Z	GPIO pin or SD card interface data bus
22	GPIO18/SDDAT1	IO,S	Z	GPIO pin or SD card interface data bus
23	GPIO19/SDDAT0	IO,S	Z	GPIO pin or SD card interface data bus
24	GPIO20/SDCMD_DI/ROT2IP0	IO,S	Z	GPIO pin, SD card interface command or rotary switch decoder input
25	GPIO21/SDCLK/ROT2IP1	IO,S	Z	GPIO pin, SD card interface clock or rotary switch decoder input
26	GPIO22/LCDCSX	IO,S	Z	GPIO pin or 6800/8080 interface chip select
27	GPIO23/LCDD[0]	IO,S	Z	GPIO pin or 6800/8080 interface data bus
28	GPIO24/LCDD[1]	IO,S	Z	GPIO pin or 6800/8080 interface data bus
29	GPIO25/LCDD[2]	IO,S	Z	GPIO pin or 6800/8080 interface data bus
30	GPIO26/LCDD[3]	IO,S	Z	GPIO pin or 6800/8080 interface data bus
31	GPIO27/LCDD[4]/I2CCK2/ROT0IP0	IO,S	Z	GPIO pin, 6800/8080 interface data bus, I2C interface clock or rotary switch decoder input
32	GPIO28/LCDD[5]/I2CSD2/ROT0IP1	IO,S	Z	GPIO pin, 6800/8080 interface data bus, I2C interface data or rotary switch decoder input
33	GPIO29/LCDD[6]/I2CCK3/ROT1IP0	IO,S	Z	GPIO pin. External LCD module interface data. LCD segment.
34	GPIO30/LCDD[7]/I2CSD3/ROT1IP1	IO,S	Z	GPIO pin. External LCD module interface data. LCD segment.
35	GPIO31/LCDWRX	IO,S	Z	GPIO pin. Emulator interface clear. LCD segment.
36	ROSCO	O	O	32.768kHz oscillator output
37	ROSCI	I	I	32.768kHz oscillator input
38	VCC	-	-	3.3V power supply
39	GND	-	-	System ground
40	GPIO32/LCDRDX	IO,S	Z	GPIO pin or 6800/8080 interface read signal
41	GPIO33/LCDA0	IO,S	Z	GPIO pin or 6800/8080 interface A0 signal
42	GPIO34/DP	IO,S	Z	GPIO pin or USB interface D+ signal
43	GPIO35/DM	IO,S	Z	GPIO pin or USB interface D- signal
44	GPIO36/I2CCK0	IO,S	Z	GPIO pin or I2C interface clock

LQFP64	Name	Type	RS	Descriptions
45	GPIO37/I2CSD0	IO,S	Z	GPIO pin or I2C interface data
46	GPIO38/REMO	IO,S	Z	GPIO pin or remote decoder input
47	GPIO39/SPICLK/EXTIRQ4/TX	IO,S	Z	GPIO pin, SPI interface clock, external interrupt input or UART transmit output (TX)
48	GPIO40/SPISDI/EXTIRQ5/RX	IO,S	Z	GPIO pin, SPI interface serial data input, external interrupt input or UART receiver input (RX)
49	GPIO41/SPISDO/EXTIRQ6/ROT2IP0	IO,S	Z	GPIO pin, SPI interface serial data output, external interrupt input or rotary switch decoder input
50	GPIO42/SPICSB/EXTIRQ7/ROT2IP1	IO,S	Z	GPIO pin, SPI interface chip select output, external interrupt input or rotary switch decoder input
51	GPIO43/I2CCK1	IO,S	Z	GPIO pin or I2C interface clock
52	GPIO44/I2CSD1	IO,S	Z	GPIO pin or I2C interface data
53	GPIO45/PWM0/DAUDI	IO,S	Z	GPIO pin, PWM output or digital audio interface data input
54	GPIO46/PWM1/BUZZER/RCCK	IO,S	Z	GPIO pin, PWM output, buzzer output or internal RC oscillator clock output
55	GPIO47/PWM2/CLK32KO/BUAD16X	IO,S	Z	GPIO pin, PWM output, 32.768kHz clock output or UART 16x baud clock output
56	TESTB	IS	PU	Test mode configuration pin with internal pull-up resistor
57	VREF	OA	PD	DAC analog reference voltage output
58	AGND	-	-	DAC analog ground
59	AVCC	-	-	DAC 3.3V analog supply
60	LOUT	OA	Z	DAC audio left channel output
61	ROUT	OA	Z	DAC audio right channel output
62	RSTB	IS	PU	Active low chip reset with internal pull-up resistor
63	GPIO00/ADC0/EXIRQ0	IO,S	Z	GPIO pin, ADC input or external interrupt input
64	GPIO00/ADC1/EXIRQ1	IO,S	Z	GPIO pin, ADC input or external interrupt input

I - Input pin
O - Output pin
IO - Bidirectional pin
IA - Analog input pin
OA - Analog output pin

S - CMOS Schmitt Trigger
Z - High impedance Z
PU - Pull up PU
PD - Pull down

8. ELECTRICAL SPECIFICATION

8.1. Absolute Maximum Rating

Item	Symbol	Rating	Unit
Power Supply Voltage (VCC)	VCC	-0.5 to 6.0	V
Analog Supply Voltage (AVCC)	AVCC	-0.5 to 6.0	V
Core Supply Voltage (VDD)	VDD	-0.5 to 6.0	V
Input Voltage	V_{IN}	-0.5 to VCC+ 0.5	V
Power Dissipation (Ta = 70℃)	Pd	TBD	mW
Storage Temperature	T_{STG}	-40 to 125	℃
Operating Temperature	T_{OPR}	0 to 80	℃

8.2. Recommended Operating Condition

Item	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage (VCC)	VCC	3.0	3.3	3.6	V
Power supply voltage (AVCC)	AVCC	3.0	3.3	3.6	V
Power supply voltage (VDD)	VDD	1.62	1.8	1.98	V
Input voltage	V_{IN}	0	-	VCC	V
Operating temperature	T_{OPR}	0	-	80	℃

8.3. Leakage Current and Capacitance

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{IN}	Input current	No pull-up or pull-down	-10	-	10	μA
I_{OZ}	Tri-state leakage current		-10	-	10	μA
C_{IN}	Input pin capacitance			8		pF
C_{OUT}	Output pin capacitance			8		pF
C_{BID}	Bidirectional pin capacitance			8		pF

8.4. DC Electrical Characteristics

(VCC=3.3V±10%, AVCC=3.3V±10%, operating temperature = 0°C-80°C, unless otherwise specified)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
GPIO buffer						
V_{IH}	Input high voltage	-	0.6*VCC	-	-	V
V_{IL}	Input low voltage	-	-	-	0.4*VCC	V
R_{PU}	Pull-up resistance GPIO and TESTB pins	V_{IN} = 0V		50		kΩ
I_{OL}	Output low current	V_{OL} = 0.4V		4		mA
I_{OH}	Output high current	V_{OH} = VCC - 0.4V		4		mA
I_{OL}	Output low current	V_{OL} = 0.4V		4		mA
1.8V LDO						
V_{DD}	Output voltage	Load current = 35mA		1.8		V
V_{DROP}	Dropout voltage	Load current = 35mA *Note 1*			100	mV
$\triangle V_{DD}$	Line Regulation	V_{CC}= 2V to 3.6V			0.3	%
$\triangle V_{DD}$	Load Regulation	Load current = 1mA to 35mA			0.3	mV/mA

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
12-bit ADC						
V_{IN}	Full scale input span		0		VCC	V
INL	Integral linearity error	Use VCC as ADC reference			±3	LSB
DNL	Differential linearity error				±1	LSB
V_{offset}	Input offset error			±5		mV
16-bit Audio DAC						
V_{FS}	Full scale output voltage	Into 10kohm, AVCC = 3.3V		-2		dBV
SNR	Signal to noise ratio	A-weighted over 20kHz bandwidth		90		dB
Current Consumption (sum of current draw at VCC and AVCC)						
Idd_opr	Operating current	*Note 2*	-	35	-	mA
Idd_rtc	Real time clock current	*Note 3*	-	-	100	µA
Idd_stdby	Standby current	*Note 4*	-	-	100	µA

Note:

1 This is simulation data only.

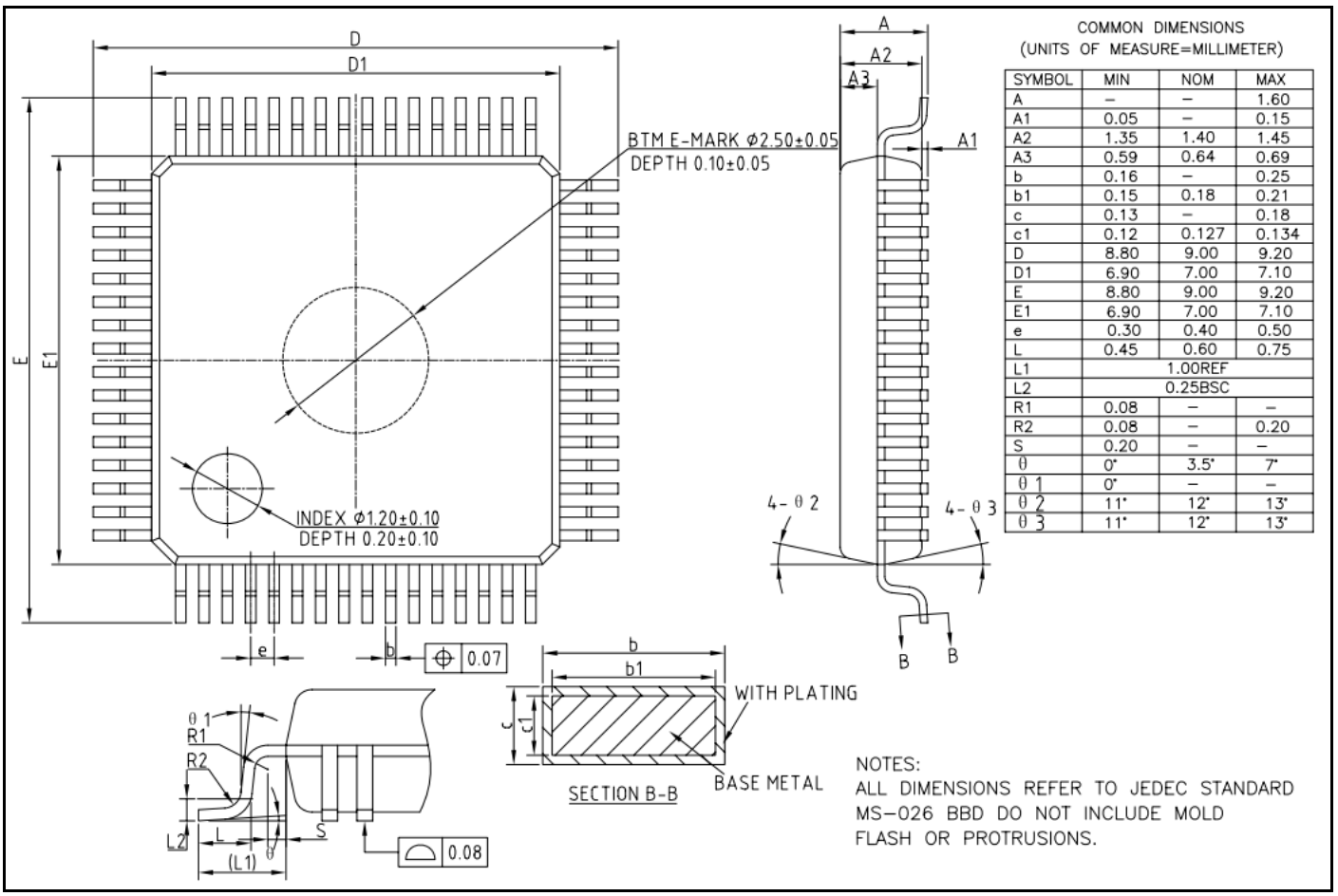
2 No load on all pins, LDO enabled, MCU run at 12MHz, ADC enabled, PLL enabled, DSP decoding MP3, Audio DAC enabled

3 No load on all pins, LDO enabled, CPU clock source use RCOSC, RTC running, ADC disabled, DAC disabled, PLL disabled, USB suspend, DSP disabled, 12MHz oscillator disabled, short flash read pulse enabled, use timer interrupt to wake up CPU.

4 All oscillator disabled, USB suspend, ADC disabled, DAC disabled, PLL disabled, USB suspend, DSP disabled, all GPIO pins output drive H

9. PACKAGE INFORMATION

64-LQFP



SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.16	–	0.25
b1	0.15	0.18	0.21
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.30	0.40	0.50
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026 BBD DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

10. SOLDERING INDICATION

This section gives a very brief insight to a complex technology. There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

1. Reflow Soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stenciling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250°C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

2. Wave Soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used, the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch:
  – Larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  – Smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45 ° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250°C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

3. Manual Soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

4. Suitability of Surface Mount IC Packages for Wave and Reflow Soldering Methods

Package	Soldering Method	
	Wave	Reflow (1)
BGA, HBGA, LFBGA, SQFP, TFBGA	Not suitable (2)	Suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	Not suitable	Suitable
PLCC (3), SO, SOJ	Suitable	Suitable
LQFP, QFP, TQFP	Not recommended (3)(4)	Suitable
SSOP, TSSOP, VSO	Not recommended (5)	Suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect).
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, the package must be placed at a 45 ° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch equal to or smaller than 0.5 mm.

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