AP702

USB Host and PLL Interface with DSP and MCU Controller

Data Sheet

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1. OVERVIEW

AP702 is an USB Host and PLL Interface with DSP and MCU Controller. It has a built-in 24-bit DSP for MP3 and WMA decoding, an 8-bit MCU for CD servo control, ISO9660 file system handling and user interface function control. An USB host controller is included in AP702 to support the data control and playback of MP3 files on portable MP3 players. AP702 also offers SD card support, giving the end customers a luxury of a SD card plug-and-play element. This chip also has an on-chip PLL controller for external tuner IC to form a complete digital tuning system. This system-on-chip solution is ideal for CD-base audio products

2. APPLICATIONS

- Micro or mini stereo sound system
- iPod docking system
- Boom box

3. FEATURES

CD Servo Interface and Control

- Interface to external CD servo controller
- Built-in CD ROM C3 ECC and EDC error detection and correction

MP2 Decoding

- Support 11.025/32/48/44.1/48kHz sampling frequencies and bit rate from 32kbps to 320kbps
- Support mono and stereo audio playback
- Support 22.05/24KHz sampling frequencies and bit rate from 8kbps to 160kbps

MP3 Decoding

- Support 16/22.05/24/32/44.1/48kHz sampling frequencies and bit rate from 32kbps to 320kbps
- Support single channel, dual channel, stereo, and joint stereo audio playback
- Support any combination of intensity stereo and MS stereo
- Support MP3 ID3 version up to version 2.4

MP3 Encoding

- Support 44.1kHz sampling frequency and bit rate from 64kbps to 128kbps
- Support stereo audio encoding
- 1x encode speed

WMA Decoding

- Support 32/44.1/48kHz sampling frequencies and bit rates of 64kbps to 320kbps
- Support single channel, dual channel, stereo, and joint stereo audio playback

USB Host and SD Card Support

- Support direct connection of USB mass storage class device into the system, such as portable MP3 player and USB flash drive
- USB card reader support
- Normal, Mini Micro SD Card support
- SDHC SD Card support
- Support FAT 12, 16 and 32 file system

4. ORDERING INFORMATION

Ordering Number	Pins	Package
AP702-LQ-L	128	LQFP

5. BLOCK DIAGRAM

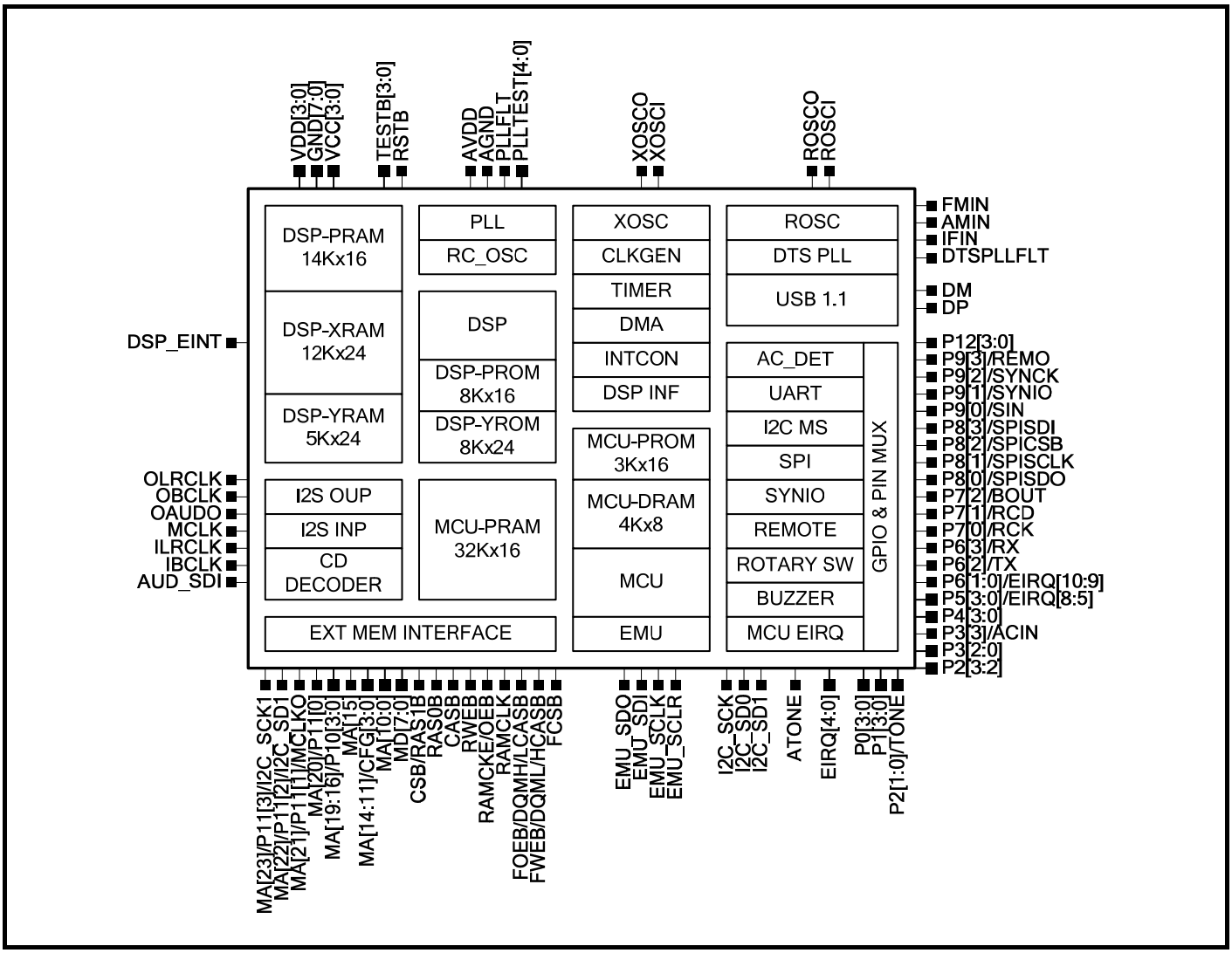

Figure 1. Block Diagram of AP702

6. PIN CONFIGURATION

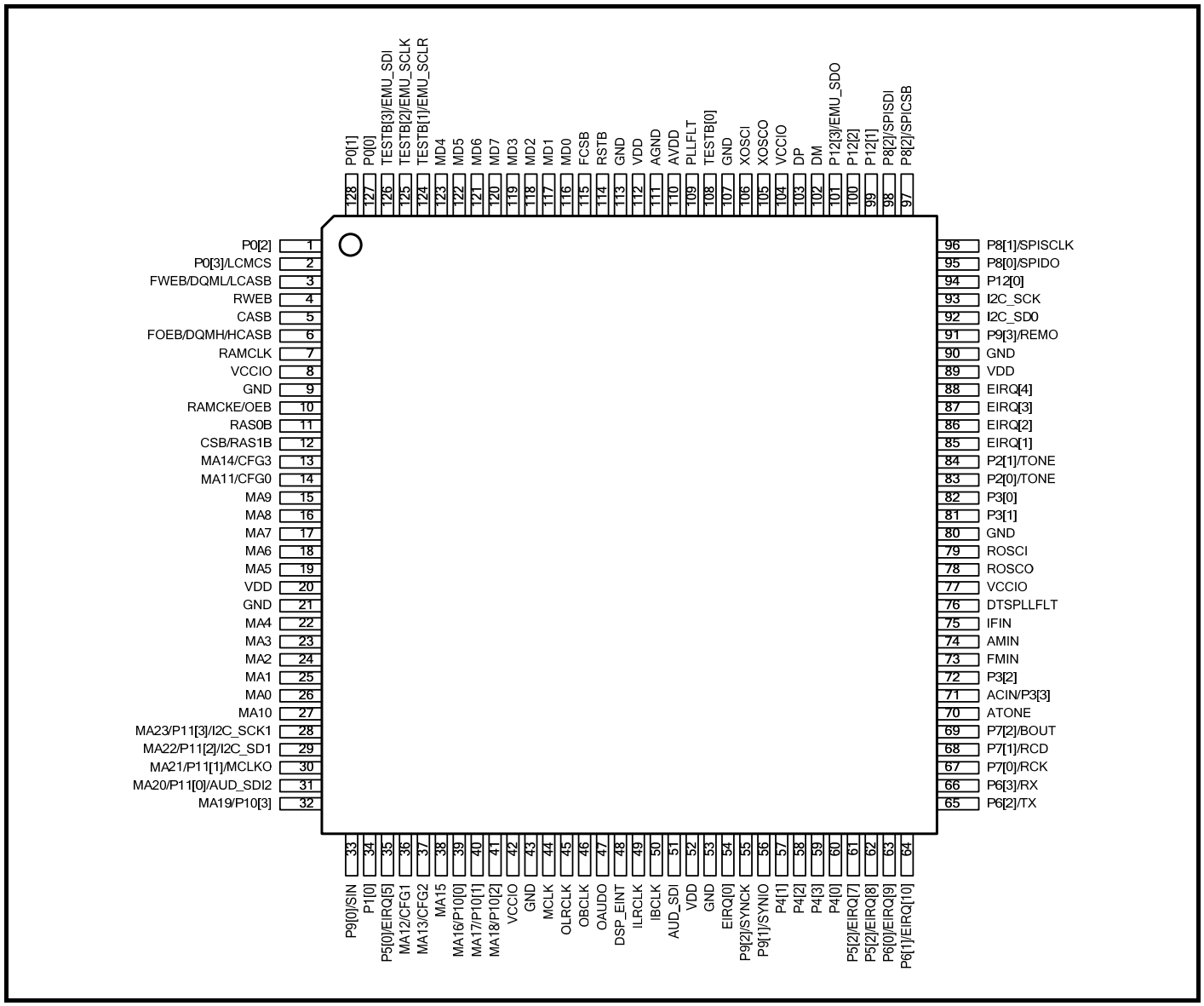

Figure 2. 128 Pin LQFP Package of AP702

7. DEVICE PIN DESCRIPTION

Pin No.	Name	Type	Drive (mA)	Descriptions
1	P0[2]	IO	4	General purpose IO port
2	P0[3]/LCMCS	IO	4	General purpose IO port or LCM chip select
3	FWEB/DQML/LCASB	O	8	1. WEB for NOR-Flash 2. DQML for SDRAM 3. CASB for EDO
4	RWEB	O	8	1. WEB for SDRAM or EDO 2. WEB for NOR Flash
5	CASB	O	8	CASB for SDRAM
6	FOEB/DQHM/HCASB	O	8	1. OEB for NOR-Flash 2. DQMH for SDRAM 3. HCASB for 16-bit EDO

Pin No.	Name	Type	Drive (mA)	Descriptions
7	RAMCLK	O	8	SDRAM operating clock
8	VCCIO	-	-	3.3V IO power supply
9	GND	-	-	Ground
10	RAMCKE/OEB	O	8	1. CKE for SDRAM 2. OEB for EDO
11	RAS0B	O	8	RASB for SDRAM or EDO
12	CSB/RAS1B	O	8	1. CSB for SDRAM 2. RASB for 2nd EDO device
13	MA14/CFG3	O	8	Memory address and reset options control bits
14	MA11/CFG0	O	8	Memory address and reset options control bits
15	MA9	O	8	Memory address
16	MA8	O	8	Memory address
17	MA7	O	8	Memory address
18	MA6	O	8	Memory address
19	MA5	O	8	Memory address
20	VDD			1.8V core supply
21	GND			Ground
22	MA4	O	8	Memory address
23	MA3	O	8	Memory address
24	MA2	O	8	Memory address
25	MA1	O	8	Memory address
26	MA0	O	8	Memory address
27	MA10	O	8	Memory address
28	MA23/P11[3]/I2C_SCK1	IO	8	1. Memory address 2. General IO port pin 3. I2C clock output
29	MA22/P11[2]/I2C_SD1	IO	8	1. Memory address 2. General IO port pin 3. I2C clock output
30	MA21/P11[1]/MCLKO	IO	8	1. Memory address 2. General IO port pin 3. 16.9344MHz clock output
31	MA20/P11[0]/AUD_SDI2	IO	8	Memory address or general IO port pin or external ADC audio data input
32	MA19/P10[3]	IO	8	Memory address or general IO port pin
33	P9[0]/SIN	IO	4	General IO port pin or synchronous interface data input
34	P1[0]	IO	4	General purpose IO port
35	P5[0]/EIRQ[5]	IO	4	General purpose IO port or MCU external interrupt input
36	MA12/CFG1	O	8	Memory address and reset options control bits
37	MA13/CFG2	O	8	Memory address and reset options control bits
38	MA15	O	8	Memory address
39	MA16/P10[0]	IO	8	General purpose IO port or memory address.
40	MA17/P10[1]	IO	8	General purpose IO port or memory address.
41	MA18/P10[2]	IO	8	General purpose IO port or memory address.
42	VCCIO			3.3V IO power supply
43	GND			Ground
44	MCLK	IO	4	16.9344MHz output clock to external DAC or ADC
45	OLRCLK	IO	4	Sampling clock for external DAC or ADC
46	OBCLK	IO	4	Bit clock for external DAC or ADC
47	OAUDO	IO	4	Serial data for external DAC or ADC
48	DSP_EINT	I	-	DSP external interrupt input
49	ILRCLK	I	-	Sampling clock input
50	IBCLK	I	-	Bit clock input
51	AUD_SDI	I	-	Audio data input
52	VDD			1.8V core supply
53	GND			Ground
54	EIRQ[0]	I	-	MCU external interrupt input pin
55	P9[2]/SYNCK	IO	4	General purpose IO port or synchronous serial interface clock output
56	P9[1]/SYNIO	IO	4	General purpose IO port or synchronous serial interface bidirectional data
57	P4[1]	IO	4	General purpose IO port
58	P4[2]	IO	4	General purpose IO port
59	P4[3]	IO	4	General purpose IO port
60	P4[0]	IO	4	General purpose IO port
61	P5[2]/EIRQ[7]	IO	4	General purpose IO port or MCU external interrupt input
62	P5[3]/EIRQ[8]	IO	4	General purpose IO port or MCU external interrupt input
63	P6[0]/EIRQ[9]	IO	4	General purpose IO port or MCU external interrupt input
64	P6[1]/EIRQ[10]	IO	4	General purpose IO port or MCU external interrupt input

Pin No.	Name	Type	Drive (mA)	Descriptions
65	P6[2]/TX	IO	4	General purpose IO port or UART TX output
66	P6[3]/RX	IO	4	General purpose IO port pin or UART RX input
67	P7[0]/RCK	IO	4	General purpose IO port pin or rotary switch counter input
68	P7[1]/RCD	IO	4	General purpose IO port pin or rotary switch counter input
69	P7[2]/BOUT	IO	4	General purpose IO port pin or UART clock output
70	ATONE	A	-	Buzzer output with level control
71	P3[3]/ACIN	IO	4	General purpose IO port pin or 50/60Hz AC detection input
72	P3[2]	IO	4	General purpose IO port pin
73	FMIN	I	-	FM input clock
74	AMIN	I	-	AM input clock
75	IFIN	I	-	IF input clock
76	DTSPLLFLT	IO	4	DTS PLL control voltage output
77	VCCIO			3.3V IO power supply
78	ROSCO	O	-	75kHz oscillator output
79	ROSCI	I	-	75kHz oscillator input
80	GND			Ground
81	P3[1]	IO	4	General purpose IO port pin
82	P3[0]	IO	4	General purpose IO port pin
83	P2[0]/TONE	IO	4	General purpose IO port pin or buzzer output
84	P2[1]/TONE	IO	4	General purpose IO port pin or buzzer output
85	EIRQ[1]	I	-	MCU external interrupt input pin
86	EIRQ[2]	I	-	MCU external interrupt input pin
87	EIRQ[3]	I	-	MCU external interrupt input pin
88	EIRQ[4]	I	-	MCU external interrupt input pin
89	VDD			1.8V core supply
90	GND			Ground
91	P9[3]/REMO	IO	4	General purpose IO port pin or remote receiver input
92	I2C_SD0	IO	4	I2C bus data
93	I2C_SCK	IO	4	I2C bus clock
94	P12[0]	IO	4	General purpose IO port pin
95	P8[0]/SPIDO	IO	4	General purpose IO port pin or SPI data output
96	P8[1]/SPISCLK	IO	4	General purpose IO port pin or SPI clock
97	P8[2]/SPICSB	IO	4	General purpose IO port pin or SPI chip select
98	P8[3]/SPISDI	IO	4	General purpose IO port pin or SPI data input
99	P12[1]	IO	4	General purpose IO port pin
100	P12[2]	IO	4	General purpose IO port pin
101	P12[3]/EMU_SDO	IO	4	General purpose IO port pin or emulator data output
102	DM	IO		USB transceiver negative data pin
103	DP	IO		USB transceiver positive data pin
104	VCCIO			3.3V IO power supply
105	XOSCO	O		16.9344MHz oscillator output
106	XOSCI	I		16.9344MHz oscillator input
107	GND			Ground
108	TESTB[0]	I	-	Active low chip test enable
109	PLLFLT	A	-	PLL filter
110	AVDD			1.8V supply for PLL
111	AGND			Analog ground for PLL
112	VDD			1.8V core supply
113	GND			Ground
114	RSTB	I	-	Active low chip reset input
115	FCSB	O	8	Flash chip select
116	MD0	IO	8	Memory data bus
117	MD1	IO	8	Memory data bus
118	MD2	IO	8	Memory data bus
119	MD3	IO	8	Memory data bus
120	MD7	IO	8	Memory data bus
121	MD6	IO	8	Memory data bus
122	MD5	IO	8	Memory data bus
123	MD4	IO	8	Memory data bus
124	TESTB[1]/EMU_SCLR	I	-	Active low chip test enable or emulator reset input
125	TESTB[2]/EMU_SCLK	I	-	Active low chip test enable or emulator data clock input
126	TESTB[3]/EMU_SDI	I	-	Active low chip test enable or emulator serial data input
127	P0[0]	IO	4	General purpose IO port
128	P0[1]	IO	4	General purpose IO port

8. EXTERNAL MEMORY CONFIGURATION

8.1 Supporting Memory Devices

Memory Device	Configurations			Number of support device
	4 bits	8 bits	16 bits	
NOR Flash	-	64k x 8	-	1
		128k x 8		
		256k x 8		
		512k x 8		
		1M x 8		
SDRAM	-	2M x 8	1M x 16	1
		8M x 8	4M x 16	
		16M x 8	8M x 16	
		32M x 8	16M x 16	
EDO	1M x 4	512k x 8	-	2
	4M x 4	2M x 8		

8.2 External Memory Connection

QFP128 Pin No.	Pin Name	Data RAM		NOR Flash	LCM
		SDRAM	EDO		
115	FCSB			CS#	
116	MD[0]	D0/D8	D0	D0	D0
117	MD[1]	D1/D9	D1	D1	D1
118	MD[2]	D2/D10	D2	D2	D2
119	MD[3]	D3/D11	D3	D3	D3
120	MD[7]	D7/D15	D7	D7	D7
121	MD[6]	D6/D14	D6	D6	D6
122	MD[5]	D5/D13	D5	D5	D5
123	MD[4]	D4/D12	D4	D4	D4
2	P0[3]/LCMCS				CS
3	FWEB/DQML/LCASB	DQML	CAS#	WE#	
4	RWEB	WE#			
5	CASB	CAS#			
6	FOEB/DQHM/HCASB	DQMH	CAS#	OE#	
7	RAMCLK	CLK			
10	RAMCKE/OEB	CKE	OE#		
11	RAS0B	RAS#	RAS# (device 1)		
12	CSB/RAS1B	CS#	RAS# (device 2)		
13	MA14/CFG3			A14	
14	MA11/CFG0	A11		A11	
15	MA9	A9	A9	A9	
16	MA8	A8	A8	A8	
17	MA7	A7	A7	A7	
18	MA6	A6	A6	A6	
19	MA5	A5	A5	A5	
22	MA4	A4	A4	A4	
23	MA3	A3	A3	A3	
24	MA2	A2	A2	A2	
25	MA1	A1	A1	A1	
26	MA0	A0	A0	A0	A0
27	MA10	A10	A10	A10	
36	MA12/CFG1	A12 (BA1)		A12	
37	MA13/CFG2	A13 (BA0)		A13	
38	MA15			A15	
39	MA16/P10[0]			A16	
40	MA17/P10[1]			A17	
41	MA18/P10[2]			A18	

9. ELECTRICAL SPECIFICATION

9.1 Absolute Maximum Ratings

Under no circumstances the absolute maximum ratings given below should be violated.
Caution: exceeding one or more of the limiting values may cause permanent damage to the device.

Parameter	Symbol	Rating	Unit
Power Supply Voltage (IO)	VCCIO	-0.3 to 4.0	V
Power Supply Voltage (Core)	VDD	-0.3 to 2.16	V
Power Supply Voltage (analog)	AVDD	-0.3 to 2.16	V
Input Voltage	V_{IN}	-0.3 to 4.0	V
Power Dissipation (Ta = 70°C)	P_d	TBD	mW
Storage Temperature	T_{STG}	-40 to 150	°C
DC input current for each I/O pin	I_{IN}	20	mA
Output short circuit current for each I/O pin	I_{OUT}	20	mA

9.2 Recommended Operating Condition

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage (IO)	VCCIO	3.0	3.3	3.6	V
Power Supply Voltage (Core Logic)	VDD	1.62	1.8	1.98	V
Power Supply Voltage (Analog)	AVDD	1.62	1.8	1.98	V
Input Voltage (Digital)	V_{IN}	0	-	VCCIO	V
Input Voltage (Analog)	V_{IN}	0	-	AVDD	V
Operating Temperature	T_{OPR}	-20	-	+85	°C

9.3 Electrical Characteristics

(VCCIO=3.3V±10%, VDD=1.8V±10%, AVDD=1.8V±10%, Operating temperature = 0°C - 70°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage		2.0	-	-	V
V_{IL}	Input Low Voltage		-	-	0.8	V
R_{PU}	Pull-Up Resistance	V_{IN} = 0V, VCCIO = 3.3V	10	12	18	kΩ
V_{ina}	FMIN,AMIN,IFIN Input Voltage		150			mVpp
I_{OL}^1	Low Level Output Current for 4mA Pins	V_{OL} = 0.4V VCCIO = 3.3V		4	-	mA
I_{OL}^2	Low Level Output Current for 8mA Pins	V_{OL} = 0.4V VCCIO = 3.3V		8	-	mA
I_{OH}^1	High Level Output Current for 4mA Pins	V_{OH} = VCCIO – 0.4V VCCIO = 3.3V		4	-	mA
I_{OH}^2	High Level Output Current for 8mA Pins	V_{OH} = VCCIO – 0.4V VCCIO = 3.3V		8	-	mA
Idd_opr	Core operating Current Idd @ VDD	Full Functional Mode, DSP Run at 96 MHz	-	30	-	mA
Idd_idle	Power Down Current Idd @ VDD	STOP Mode VCCIO = 3.6V VDD = 1.98V	-	300	800	µA

10. PACKAGE INFORMATION

ALL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BASIC			0.630 BASIC		
D1	14.00 BASIC			0.552 BASIC		
E	16.00 BASIC			0.630 BASIC		
E1	14.00 BASIC			0.552 BASIC		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	0.127	0.16	0.004	0.005	0.006
L1	1.00 REF			0.039 REF		
L	0.45	0.60	0.75	0.018	0.024	0.030
S	0.20	—	—	0.008	—	—
b	0.13	—	0.23	0.005	—	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
e	0.40 BSC.			0.016 BSC.		
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

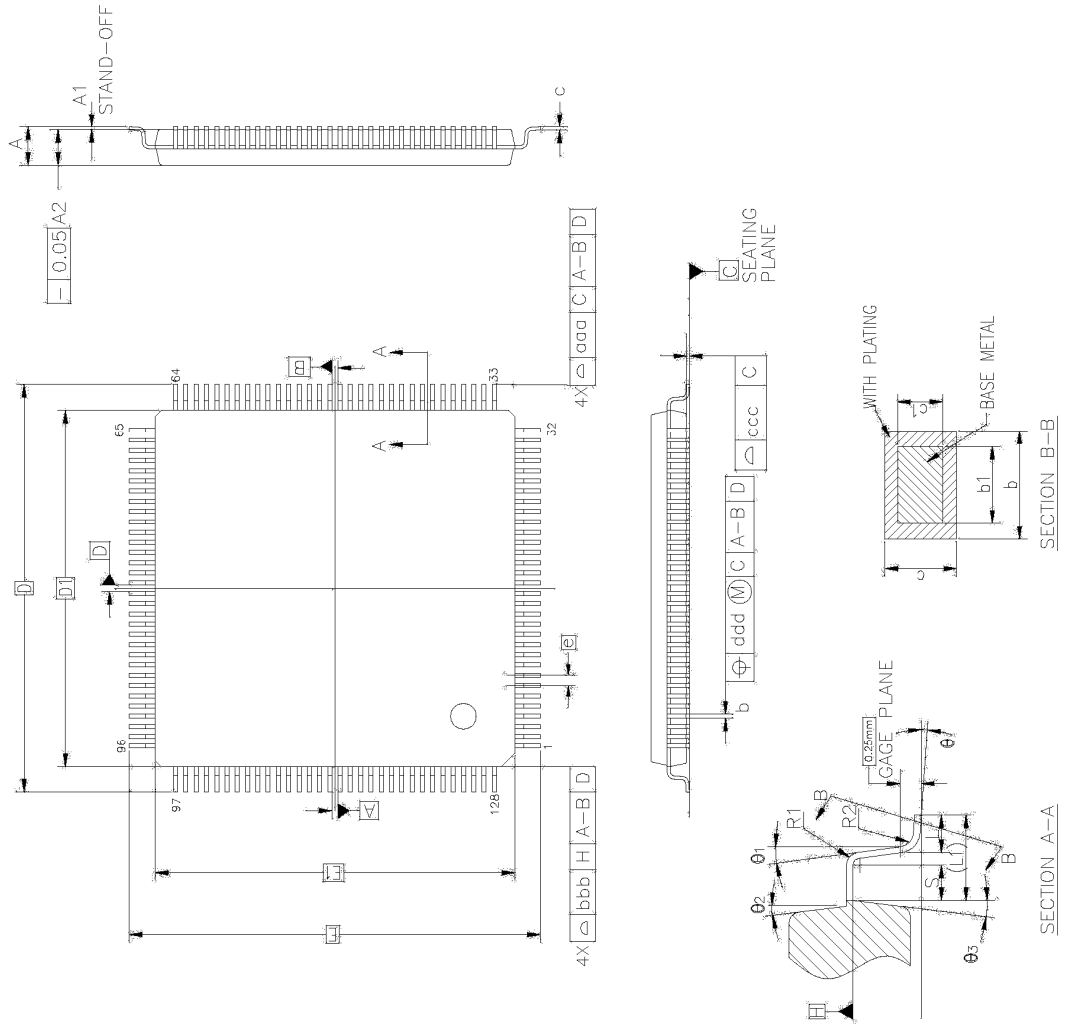

Figure 3. LQFP Package Dimension Drawing

11. SOLDERING INDICATION

This section gives a very brief insight to a complex technology. There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

1. Reflow Soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stenciling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

2. Wave Soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used, the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.

- For packages with leads on two sides and a pitch:
  – larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  – smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

3. Manual Soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

4. Suitability of Surface Mount IC Packages for Wave and Reflow Soldering Methods

Package	Soldering Method	
	Wave	Reflow (1)
BGA, HBGA, LFBGA, SQFP, TFBGA	Not suitable (2)	Suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	Not suitable	Suitable
PLCC (3), SO, SOJ	Suitable	Suitable
LQFP, QFP, TQFP	Not recommended (3)(4)	Suitable
SSOP, TSSOP, VSO	Not recommended (5)	Suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect).
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch equal to or smaller than 0.5 mm.

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